User Guide

CCM-BOOGIE • CompactPCI®

3U High Performance Core™ 2 Duo CPU Board

Document No. 5292 • Edition 19 • 4 May 2012

CCM-BOOGIE

Contents

About this Manual

This manual describes the technical aspects of the CCM-BOOGIE, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/*Changes*	Author	Date
1	User Manual CCM-BOOGIE, english, initial edition (Text #5292, File: ccm_uge.wpd)	gn	2008-10-27
2	Added 'Top View Component Assembly' diagram, changed 'Mechanical Drawings', changed LPC bridge device ID in table 'Local PCI Devices', removed section 'Mass Storage Considerations'.	gn	2008-11-07
3	Added chapter 'Mezzanine Side Board Options'	jj	11 November 2008
4	Added Images CCM-BOOGIE, Mezzanine Stack	jj	5 January 2009
5	Replaced DVI connector illustration, replaced C44-SATA illustration, table 'Literature' updated and moved to table 'Standards', minor changes throughout text/tables reflecting C42-SATA and CCO-CONCERT	jj	19 February 2009
6	Corrected SMBus Address of ADT7421. Corrected typo within CompactPCI J2 connection table. Added PCIe-SATA-Bridge JMB362 to local PCI devices table.	gn	2009-03-17
7	Added power requirements and performance rating for CCM-6 to table 'Feature Summary'. Added some images and illustrations of mezzanine modules and side cards.	gn	2009-09-01
8	Added power requirements for sleep states S3 S4 S5	jj	3 September 2009
9	Added photo CCM bottom view	jj	24 September 2009
10	Added photo CCT custom specific version, added photos CCG-CCK-DX1 exploded view, added photo CR4	jj	17 November 2009
11	CCH-MARIACHI side card replaced by CCO-CONCERT	jj	19 February 2010
12	Added to table Feature Summary: +3.3V V(I/O) option	jj	5 November 2010
13	Parallel ATA drives on side cards not supported	jj	1 March 2011
14	Added description of unlocked front panel handle signalling	gn	2011-04-13
15	Added photos showing how to force system shutdown using the front panel handle integrated switch, added photos 'Small Systems' and 'Rugged Systems'	jj	13 May 2011
16	BIOS usage of GP LED - link added	jj	18 May 2011
17	Highlighted BIOS GP LED Usage Link	gn	2011-06-17
18	Added photos of several mezzanine storage modules	jj	23 August 2011
19	Added MTBF value to table Feature Summary	gn	2012-05-04

Related Documents

For ordering information refer to document CCM-BOOGIE Product Information, available at www.ekf.com/c/ccpu/ccm/ccm_pie.pdf.

Other documents related to the CCM-BOOGIE - in particular technical information of suitable mezzanine side boards - can be found at www.ekf.com/c/ccpu/ccm/ccm_e.html.

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Pentium, Pentium M, Celeron M, Core 2 Duo, Penryn, Cantiga GS45, Montevina Platform, Boazman, Fern Hill CRB, iAMT: ® Intel
- ***CompactPCI***: ® PICMG
- Windows 2000, Windows XP, Windows Vista: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Theme	Document Title	Origin
CompactFlash	CF+ and CompactFlash Specification Revision 3.0	www.compactflash.org
CompactPCI	CompactPCI Specification, PICMG 2.0 R3.0, Oct. 1, 1999	www.picmg.org
DVI	Digital Visual Interface Rev. 1.0 Digital Display Working Group	www.ddwg.org
Ethernet	IEEE Std 802.3, 2000 Edition	standards.ieee.org
HD Audio	High Definition Audio Specification Rev.1.0	www.intel.com/design/chipsets/hdaudio.htm
PCI Express	PCI Express® Base Specification 1.1	www.pcisig.com
PCI Local Bus	PCI 2.2/2.3/3.0 Standards PCI SIG	www.pcisig.com
SATA	Serial ATA 2.5/2.6 Specification	www.sata-io.org
TPM	Trusted Platform Module 1.2	https://www.trustedcomputinggroup.org
USB	Universal Serial Bus Specification	www.usb.org

CCM-BOOGIE Features

Feature Summary

Feature Summary CCM-BOOGIE	
Form Factor	Single size *CompactPCI* style Eurocard (160x100mm²), front panel width 4HP (20.3mm)
Processor	Designed for Intel® Core™ 2 Duo SFF (Small Form Factor) processors (codename Penryn), 1066/800MHz FSB, maximum junction temperature 105°C, Enhanced Intel® Speedstep® Technology [1], Dual Core Multiprocessing [1], Intel® Virtualization Technology (VT) [1], Intel® 64 Architecture ▸ Core™ 2 SV • SP9300 • 2.26GHz • FSB 1066MHz • 6MB L2 Cache • 25W TDP ▸ Core™ 2 LV • SL9400 • 1.86GHz • FSB 1066MHz • 6MB L2 Cache • 17W TDP ▸ Core™ 2 ULV • SU9300 • 1.2GHz • FSB 800MHz • 3MB L2 Cache • 10W TDP ▸ Celeron® M ULV • 722 • 1.2GHz • FSB 800MHz • 1MB L2 Cache • 5.5W TDP [1] features not available with Celeron® M ULV 722 processor
Chipset	Mobile Intel® 45 (Codename Cantiga) chipset comprised of: ▸ GS45 Graphics/Memory Controller Hub (GMCH) with Intel® Gen. 5.0 integrated graphics engine with 10 fully-programmable cores, 1600x1200 dual independent display, HW support for H.264, MPEG2, VC-1, improved 3D capability (DirectX 10/OpenGL 2.0 support), estimated 533-MHz core render clock (low-power mode 266MHz), iAMT manageability engine, option Integrated Trusted Platform Module (ITPM) ▸ ICH9M-E Enhanced I/O Controller Hub, integrated GbE MAC, 12 x USB (2 x EHCI, 6 x UHCI cntrls.), 4 x SATA 3Gbps, Intel® Matrix Storage Technology (RAID 0, 1, 5, 10), iAMT, High Definition Audio, unified SPI Flash support
Memory (RAM)	▸ Maximum memory capacity of 8GB DDR3 up to 1066MHz ▸ 512Mb, 1Gb, 2Gb, [4Gb] technologies for x8 and x16 devices ▸ Channel 0 populated as directly soldered DDR3 devices (Memory Down) ▸ Channel 1 provided as 204-pin SODIMM socket to carry DDR3 module PC3-8500 ▸ Dual channel symmetric – memory addresses interleaved for increased performance (SODIMM module size must match Memory Down size) ▸ Intel® Flex Memory Technology (dual channel interleaved mode with unequal memory population) - memory sizes maybe unequal in both the channels ▸ Dual channel asymmetric – memory sizes may differ, including no memory module populated in the SODIMM socket (single-channel)
Non Volatile Memory (NVM)	▸ Intel® Turbo Memory card (codename Robson) on CCI-RAP mezzanine side board optionally available ▸ PCI Express Mini Card 1G Byte Flash ▸ Microsoft® ReadyDrive and ReadyBoost (Windows® Vista) ▸ Intel® Turbo Memory driver
Video	▸ Both (concurrently) analog monitor and digital flat-panel display support by DVI-I connector (front panel), up to 2048x1536 pixel 16M colours @75Hz refresh rate (analog), up to 1600 x 1200 pixel 16M colours @60Hz (digital), incorporates PanelLink Digital technology (Silicon Image) ▸ Dual screen capable 2 x 1600 x 1200 pixel (one display attached to the front panel, the other to the back panel, or both to the front panel by means of a DVI-I to DVI-D/VGA splitter cable, or secondary DVI-D connector on mezzanine side board) ▸ Front panel option: D-Sub (female HD15) VGA connector available, replaces DVI-I connector ▸ Rear I/O option: Analog video output configurable (BIOS) across J2/P2 CCT-RIO rear I/O transition module ▸ Mezzanine option: Secondary DVI-D connector at mezzanine card front panel allows for dual digital flat panel operation, suitable mezzanine modules e.g. CCH-MARIACHI, CCI-RAP, CCJ-RHYTHM, CCO-CONCERT

Feature Summary CCM-BOOGIE	
USB	▸ All ports over-current protected, data transfer rate of up to 480Mbps, conforming to USB2.0 ▸ 2 x USB type A connector (front panel) ▸ 3 x USB ports J2/P2 Rear I/O option (CCT-RIO rear I/O transition module) ▸ 2 x USB ports via J-EXP expansion interface option (in use by several mezzanine side boards) ▸ 4 x USB ports via J-HSE (C40-SCFA mezzanine storage module) ▸ Dual EHCI / six UHCI controllers provided by ICH9M-E
Ethernet	▸ Two 10/100/1000Mbps Gigabit Ethernet controllers, accessible via RJ45 jacks from the front panel ▸ ETH1 equipped with Intel® 82567LM PHY (codename Boazman), serves also as AMT out of band communication path (MAC provided by ICH9M-E), Jumbo Frame support up to 9KB ▸ ETH2 equipped with Intel® 82574L GbE controller (codename Hartwell), connected to local PCIe lane, supports 9018-byte jumbo packets, TimeSync Offload compliant with 802.1as specification ▸ Option ETH1 Gigabit Ethernet configurable (BIOS setup) across J2/P2 with attached CCT-RIO rear I/O transition module
SATA	▸ Total of six 3Gbps SATA channels available ▸ Triple-channel Serial ATA 3Gbps available for J2/P2 rear I/O option (derived from ICH9) ▸ Suitable rear I/O transition module CCT-RIO (2 x system internal SATA, 1 x eSATA for attachment of external devices) ▸ Intel® Matrix Storage Technology MST (Raid 1, 0, Matrix Raid) ▸ Secondary on-board PCIe to SATA controller JMB362, dual channel SATA RAID, available via J-HSE expansion connector (plus 1 SATA channel in addition from ICH9) ▸ Additional PCIe to SATA controller on mezzanine side boards e.g. CCI-RAP, CCK-MARIMBA, CCL-CAPELLA, CCO-CONCERT
PATA (IDE)	▸ Option mezzanine module attached to J-HSE expansion connector ▸ C40-SCFA mezzanine module available with on-board SATA to PATA bridge and CompactFlash socket
PCI Express	▸ 4-Lane PCIe high-speed connector J-PCIE for CCJ-RHYTHM and other mezzanine expansion cards (side boards) ▸ Possible configurations 1 Link x 4 Lanes, 4 Links x 1 Lane

Mezzanine Side Board I/O	▸ J-EXP Legacy expansion interface connector LPC/USB/Audio (SIO, USB, HD Audio)
	▸ J-HSE High-speed expansion interface connector (3 x SATA, 4 x USB)
	▸ J-PCIE PCI Express 4-lane high-speed expansion connector
	▸ J-SDVO secondary digital graphics port high-speed expansion connector
	▸ Suitable mezzanine companion side boards available, e.g.:
	  ▸ *CCI-RAP*: 2 x PCI Express Mini Card sockets (WLAN, GSM, Wimax, Intel® Turbo Memory), options secondary DVI-D, IEEE 1394 (FireWire), USB SSD, C20-SATA mezzanine storage module (accommodates up to 2 SATA hard disk drives 2.5-inch RAID capable)
	  ▸ *CCJ-RHYTHM*: CompactPCI Express system slot controller function by on board 6-port 24-lane PCIe switch, options DVI-D, IEEE 1394 (FireWire)
	  ▸ *CCK-MARIMBA*: PMC/XMC module carrier, option C20-SATA mezzanine storage module
	  ▸ *CCL-CAPELLA*: Up to 4 Gigabit Ethernet ports, options IEEE 1394 (FireWire), USB SSD, C20-SATA mezzanine module
	  ▸ *CCO-CONCERT*: Audio analog/digital, option secondary DVI-D
	  ▸ *C23-SATA*: PCIe to 2 x SATA 1 x PATA controller
	  ▸ *C40-SCFA*: SATA to PATA bridge & CompactFlash header, option USB SSD, 4HP envelope maintained
	  ▸ *C41-CFAST*: CFast™ Flash card header, 4HP envelope maintained
	  ▸ *C42-SATA*: 1.8-inch SATA Solid State Drive (SSD), 4HP envelope maintained

Feature Summary CCM-BOOGIE	
J2 Rear I/O	▸ Suitable rear I/O transition module CCT-RIO available ▸ 3 x Serial ATA (SATA), 2 x system internal SATA connectors, 1 x external eSATA connector ▸ 1 x Gbit Ethernet (switched by BIOS between front panel I/O and rear I/O) ▸ 3 x USB ▸ VGA Analog Video (switched by BIOS between front panel I/O and rear I/O) ▸ PS/2 Keyboard, Mouse ▸ COM port (TTL Level)
J1 *CompactPCI*®	▸ ICH9M-E integrated 32-bit PCI bridge, 33MHz 133MBps CPCI master ▸ Additional PCI arbiter in PLD for fully figured 8-slot CompactPCI backplane ▸ +5V V(I/O) default configuration (PCI pull-up resistors 1k - blue coding key on J1) ▸ +3.3V V(I/O) on request (PCI pull-up resistors 2.7k - yellow coding key on J1)
CompactPCI® *Express*	▸ CCM-BOOGIE can be configured as CompactPCI Express System Board (system slot controller) by optionally available mezzanine expansion card (side board) CCJ-RHYTHM ▸ CPCIe 4-Link configuration (4-lanes each), for up to 4 CPCIe peripheral slots type 1 and/or type 2 on a passive CPCIe backplane ▸ Suitable also for hybrid CPCI/CPCIe systems/backplanes (e.g. Schroff)
CompactPCI® *Serial*	▸ CCM-BOOGIE can be configured as CompactPCI Serial System Board (system slot controller) by optionally available mezzanine expansion card (side board) SJ1-JAM ▸ Suitable for hybrid CompactPCI and CompactPCI Serial systems/backplanes
Platform Management (on Request)	▸ *Hardware is ready for AMT 4.0 Intel® Active Management Technology (iAMT)* ▸ *ARM core based Manageability Engine (ME) in the GMCH* ▸ *Independent manageability firmware, to be stored in SPI Flash* ▸ *No iAMT BIOS support available as of current*
Secure Computing	▸ Option Trusted Platform Module TPM 1.2 according to Trusted Computing Group specifications ▸ Choose from either integrated solution (GS45 Intel® Trusted Execution Technology), or available as discrete controller on several mezzanine boards e.g. CCH/CCI/CCJ ▸ Discrete crypto engine silicon brands Infineon or Atmel at users choice
BIOS	▸ Phoenix BIOS with EKF enhancements for embedded systems ▸ SPI Flash memory 2 x 16/32/64 Mb ▸ Updates available from website ekf.com
Drivers (All Major OS)	▸ Intel® graphics driver, Intel® embedded graphics driver ▸ Intel® networking driver ▸ Intel® Matrix Storage Manager software ▸ Intel® Turbo Memory driver ▸ JMicron SATA driver
Thermal Conditions Environmental Conditions	▸ Operating temperature: 0°C ... +70°C (CPU dependent) ▸ Storage temperature: -40°C ... +85°C, max. gradient 5°C/min ▸ Humidity 5% ... 95% RH non condensing ▸ Altitude -300m ... +3000m ▸ Shock 15g 0.33ms, 6g 6ms ▸ Vibration 1g 5-2000Hz
EC Regulations	▸ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▸ 2002/95/EC (RoHS)
MTBF	141 x 10^3 h (16 years) @ 50° C

<table>
<tr><td rowspan="4">Typical Power Requirements

1) Intel® SpeedStep® Frequency Modes LFM: Low Frequency Mode, HFM: High Frequency Mode

2) Add per Ethernet port 0.4/1.2A (link only/active) @1Gbps or 0.1/0.4A @ 100Mbps</td><td rowspan="2">Board</td><td colspan="2">+3.3V +0.17V/-0.1V</td><td colspan="2">+5V +0.25V/-0.15V</td></tr>
<tr><td>MaxPower LFM/HFM 1)</td><td>WinXP Idle LFM/HFM 1)</td><td>MaxPower LFM/HFM 1)</td><td>WinXP Idle LFM/HFM 1)</td></tr>
<tr><td rowspan="2">CCM-6-BOOGIE</td><td>5.1/5.2A 2)</td><td>2.1/2.1A 2)</td><td>2.3/4.5A</td><td>0.3/0.5A</td></tr>
<tr><td colspan="2">S3: 200mA
S4: 100mA
S5: 100mA</td><td colspan="2">S3: 50mA
S4: 50mA
S5: 30mA</td></tr>
<tr><td rowspan="4">Performance Rating

Measured with PCMark2005 under Windows XP, 2 x 2GB DDR3 1066</td><td>Board</td><td colspan="2">Processor</td><td colspan="2">CPU/MEM Score</td></tr>
<tr><td>CCM-6-BOOGIE</td><td colspan="2">SP9300</td><td colspan="2">5650</td></tr>
<tr><td>CCM-4-BOOGIE</td><td colspan="2">SL9400</td><td colspan="2"></td></tr>
<tr><td>CCM-2-BOOGIE</td><td colspan="2">SU9300</td><td colspan="2"></td></tr>
</table>

Table items are subject to technical changes

Short Description CCM-BOOGIE

*The CCM-BOOGIE is a versatile 4HP/3U **CompactPCI®** CPU board, equipped with an Intel® Core™ 2 Duo processor at up to 2.26GHz clock, and up to 8GB dual channel capable DDR3 RAM. Four native 3Gbps RAID capable Serial ATA channels are available for mass storage I/O, and in addition another two from a secondary RAID controller. The CCM-BOOGIE has been designed especially for systems which require dual core high performance at moderate power consumption.*

The CCM-BOOGIE is provided with a high performance mobile chipset (Intel® GS45) which operates at up to 1066MHz FSB and up to 1066MHz DDR3 memory clock for optimum system throughput. The chipset is based on PCI Express® technology and has a powerful integrated graphics accelerator. The DVI-I front panel connector enables dual screen video operation. Two Gigabit Ethernet controllers are provided for high speed connectivity (one of them IEEE 802.1as TimeSync compliant).

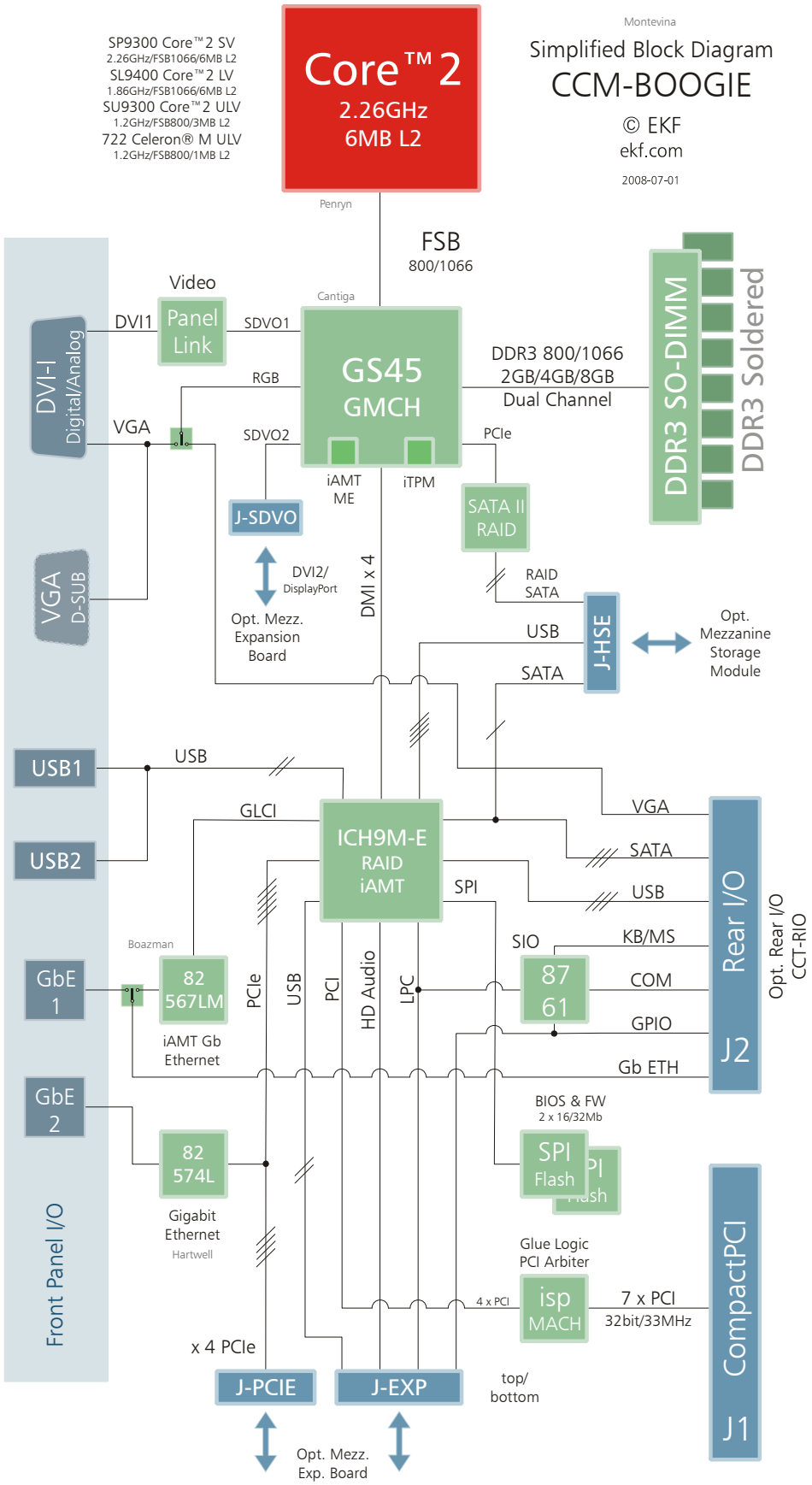
The CCM-BOOGIE is equipped wit a set of local expansion interface connectors, which can be optionally used to directly attach a suitable (application specific) mezzanine side board, e.g. for audio- and legacy support, PCI Express based I/O circuitry, and a secondary DVI video output. Carrier board and side card come as a readily assembled 8HP unit typically. Most mezzanine cards can accommodate in addition a 2.5-inch drive. Also as an option, a suitable rear I/O transition module is available to the CCM-BOOGIE.

As a popular add-on option, the CCM-BOOGIE can be delivered with a small mezzanine module (C42-SATA), which accommodates a 1.8-inch SATA solid state drive (SSD). Alternatively, the C40-SCFA mezzanine card is provided with an industrial grade CompactFlash memory card, and/or an even more rugged USB Silicon State Drive (SSD). Both mezzanine modules fit into the 4HP envelope of the entire assembly.

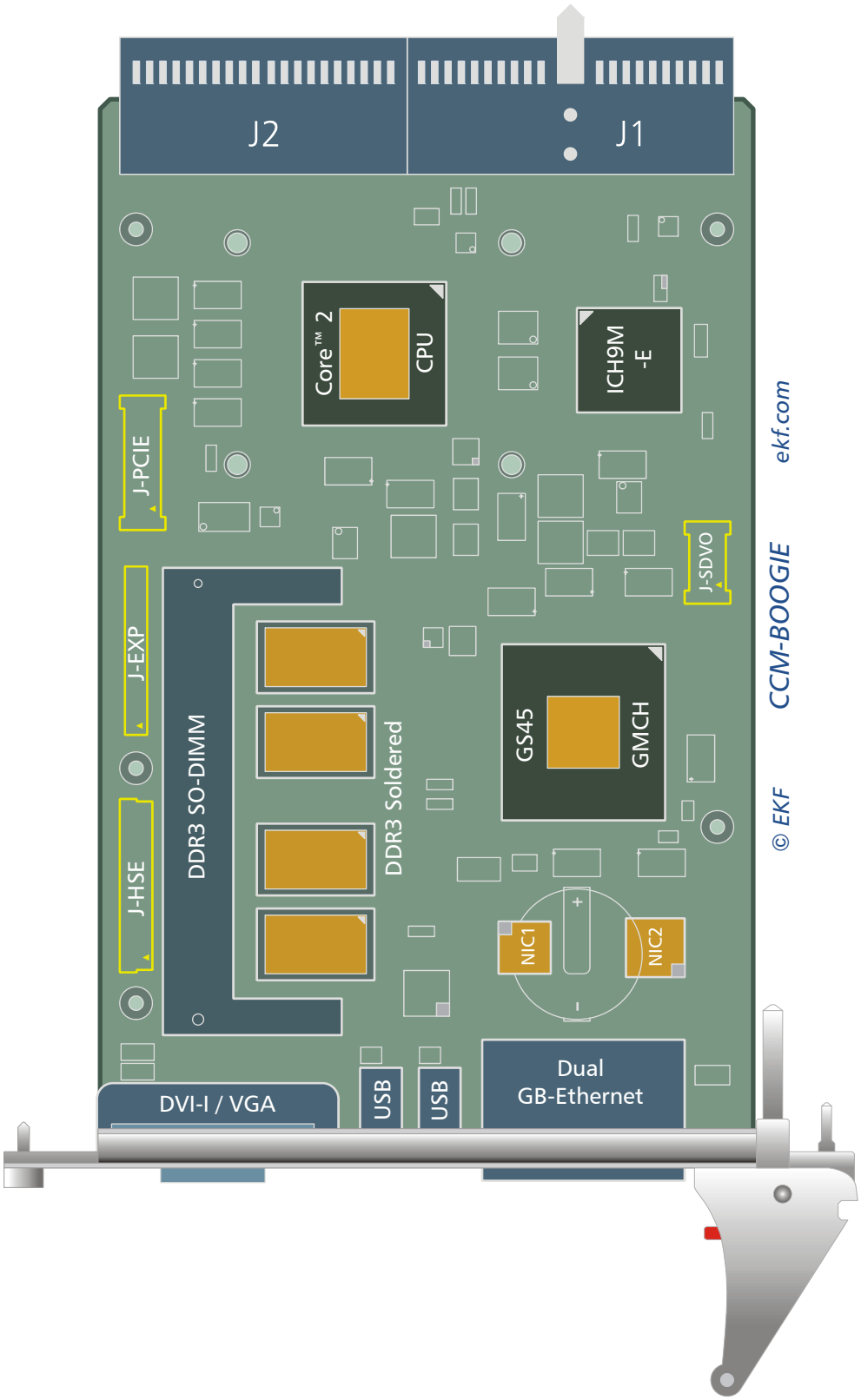
Benefits of the CCM-BOOGIE

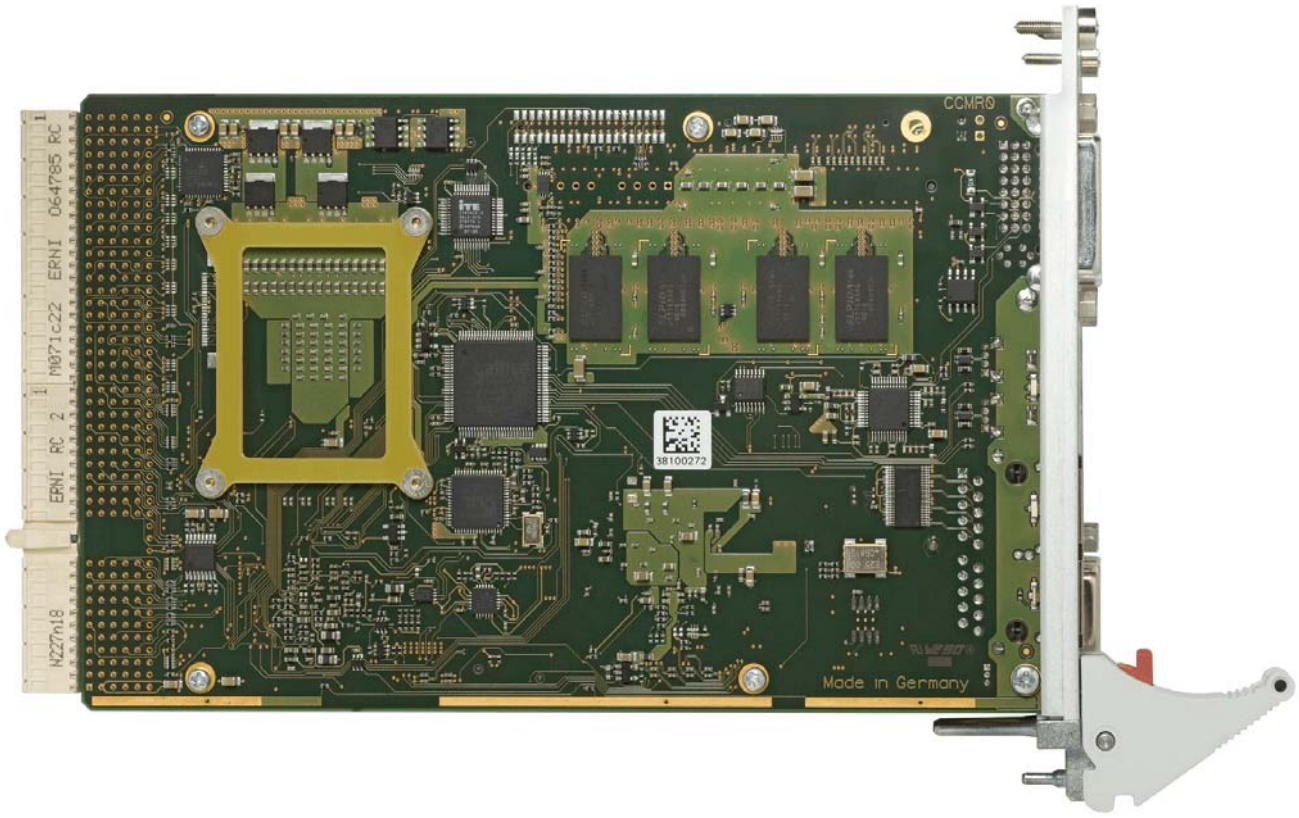
- High Performance *CompactPCI®* System Slot Controller with or w/o Rear I/O
- *CompactPCI® Express* System Board Option (CCJ-RHYTHM Mezzanine Expansion Card)
- Hybrid Systems Option (Dual Backplane *CompactPCI®* & *CompactPCI® Express*)
- *Intel® Core™ 2 Duo SV* (45nm Penryn) Mobile Processor 2.26GHz 6MB L2 Cache (FSB 1066MHz)
- Scalable Series of Small Form Factor (SFF) Processors from 1.2GHz to 2.26GHz
- PCI Express Mobile Intel® 45 Express Chipset GS45 (Cantiga)
- Up to 2 x 4GB DDR3 Memory (Dual Channel Mode Capable, up to 1066MHz)
- One Memory Bank Soldered (Memory Down) for Extreme Ruggedized Systems
- Dual-Screen Graphics Controller
- Dual Gigabit Ethernet Controllers
- Four Native SATA Channels 3Gbps, Intel® Matrix Raid Storage Technology
- Two Additional SATA Channels 3Gbps, RAID capable with JMicron Drivers
- Eleven USB 2.0 channels
- CompactFlash and/or USB SSD with C40-SCFA Mezzanine Module Option (4HP Maintained)
- SATA SSD 1.8-Inch with C42-SATA Mezzanine Module Option (4HP Maintained)
- Variety of Mezzanine Expansion Boards Available with and w/o PCIe
- TPM 1.2 Option (on Mezzanine Expansion Board or GS45 Internally)
- Rear I/O Transition Module Option
- Intel® AMT 4.0 Platform Management
- RoHS compliant

Block Diagram CCM-BOOGIE



Top/Bottom View Component Assembly





Bottom View CCM-BOOGIE

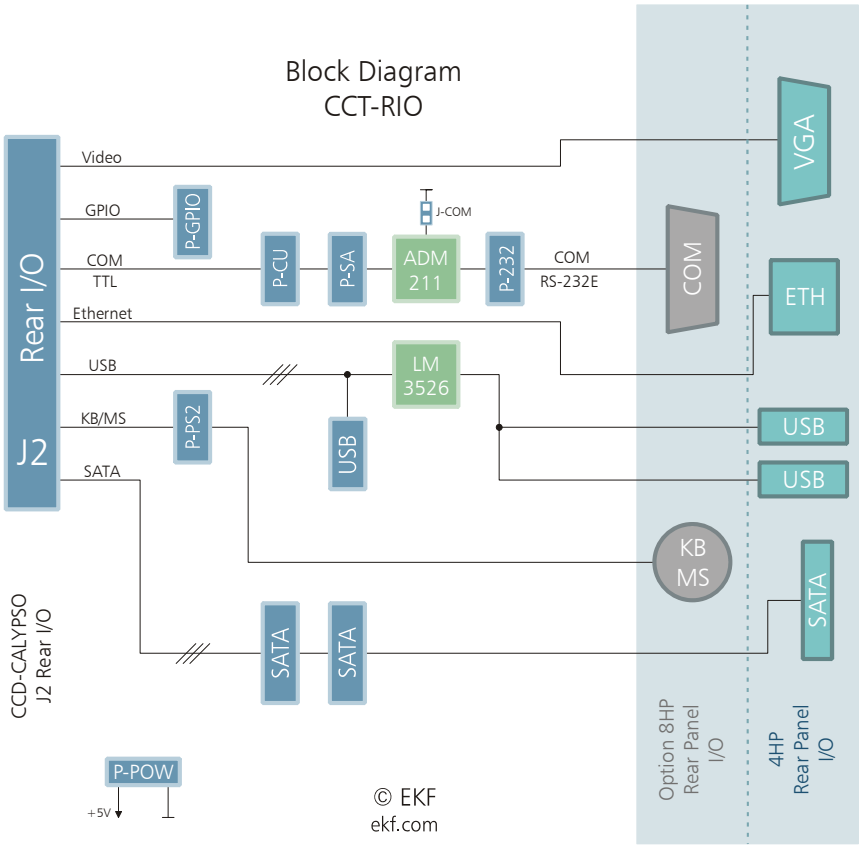
Rear I/O Transition Module CCT-RIO

Available as a rear I/O expansion board to the CCM-BOOGIE CPU card, the CCT-RIO is provided with several I/O port connectors, to be used either in addition to the CCM-BOOGIE front panel connectors or alternatively. Being mainly a passive rear I/O transition module, groups of signals from the CCM-BOOGIE CPU board are passed across the CompactPCI J2/P2 connector to the CCT-RIO. Some of the data lines are available locally on the CCT board for system internal wiring only, while other connectors such as VGA-Video and Gigabit Ethernet are mounted into the back panel for external use. USB and SATA (eSATA) channels are provided both on-board and externally.

Typically the CCT-RIO ist equipped with a 4-HP rear panel (20.3mm width). As a custom specific option, an 8-HP panel is available with additional connectors.

Utilization of the CCT-RIO transition module adds a level of I/O functionality that is not available with the CCM-BOOGIE CPU board alone. Further on, swapping the CPU card is simplified by means of rear I/O, which is important for efficient system maintenance (MTTR). Be sure to have ordered a CCM-BOOGIE rear I/O capable version and also the CPCI backplane suitable for rear I/O in order to use the CCT-RIO transition module.

CCT-RIO (Shown with on-Board USB Stick)



CCT-RIO Custom Specific Version

Strapping Headers

P_ISP	PLD Programming Connector, not stuffed
P_GP	Jumper to Reset BIOS CMOS RAM Values
P_RST	Jumper to Reset Board
P_RTC	Jumper to Reset RTC Core of ICH9, not stuffed

Connectors & Sockets

J1/J2	*CompactPCI* Bus 32-bit, 33MHz, PXI, Rear I/O
J_EXPT J_EXPB [1)]	Expansion Interface Connector (LPC Interface (2nd Super-I/O, 2nd FWH), USB Interfaces, HD Audio Interface, SMBus), available either from top (T) or bottom (B) of the board
J_HSE	High Speed Expansion Connector (2 x SATA, 4 x USB), Interface to CompactFlash Carrier C40-SCFA
XDP1	CPU Debug Port
J_PCIE	PCI Express Expansion Interface Connector
SODM1	204-pin DDR3 Memory Module SDRAM PC3-8500 Socket

[1)] Stuffed on customers request only

Front Panel Elements

Ethernet (GbE1/2)	Dual 1000Base-TX/100Base-TX/10Base-T, RJ-45 Receptacles with integrated indicator LEDs
Graphics (DVI-I)	DVI-I Integrated (digital & analog) Receptacle, suitable for DVI digital flat panel displays and/or analog monitors
USB1/2	Universal Serial Bus 2.0 self powered root hub, type A receptacle
GP	General Purpose LED
HD	LED indicating any activity on SATA ports
PG	LED indicating Power Good/Board Healthy

Microprocessor

The CCM-BOOGIE is designed for use with Core™2 Duo processors manufactured in 45nm technology (code name Penryn). These includes also the Ultra Low-Voltage (ULV) and the Low-Voltage (LV) Core™2 Duo processors as listed below. The processors are housed in a Small Form Factor (SFF) Micro FC-BGA package for direct soldering to the PCB, i.e. the CPU chip cannot be removed or changed by the user.

The processors supported by the CCM-BOOGIE are running at FSB clock speeds of 800MHz or 1066MHz. The internal Core™2 Duo processor speed is achieved by multiplying the host bus frequency by a variable value. The multiplier is chosen by currently required performance and the actual core temperature. To further lowering the power dissipation, the processor is able to halve its FSB clock speed dynamically. This technology is called Enhanced Intel SpeedStep®.

Power is applied across the *CompactPCI* connectors J1 (3.3V, 5V). The processor core voltage is generated by a switched voltage regulator, sourced from the 5V plane. The processor signals its required core voltage by 7 dedicated pins according to Intels IMVP-6 voltage regulator specification.

45nm Processors Supported									
Processor	Number of Cores	Speed min/max [GHz]	Host Bus [MHz]	L2 Cache [MB]	TDP [W]	Die Temp [°C]	CPU ID	Stepping	sSpec
ULV Celeron M 722	1	1.20/1.20	800	1	5.5	0-100	TBD	TBD	TBD
ULV Core 2 Duo SU9300	2	0.80/1.20	800	3	10	0-105	10676h	M-0	SLB5Q
LV Core 2 Duo SL9400	2	0.80/1.86	1066	6	17	0-105	10676h	C-0	SLB66
SV Core 2 Duo SP9300	2	0.80/2.26	1066	6	25	0-105	10676h	C-0	SLB63

Thermal Considerations

In order to avoid malfunctioning of the CCM-BOOGIE, take care of appropriate cooling of the processor, GMCH and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. Please note, that the processors die temperature is steadily measured by a special controller (ADT7421), attached to the onboard SMBus® (System Management Bus). The processor also contains a digital thermal sensor (DTS) that is readable via special CPU registers. DTS allows to get the temperatures of each CPU core separately.

Two further temperature sensors located in the system hardware monitor LM87 allows for acquisition of the boards surface temperature and the thermal state of the onboard system memory channel. Beside this the LM87 also monitors most of the supply voltages. A suitable software to display both, the temperatures as well as the supply voltages, is MBM (Motherboard Monitor), which can be downloaded from the web. After installation, both temperatures and voltages can be observed permanently from the Windows taskbar.

The CCM-BOOGIE is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a *CompactPCI* board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended ($>15m^3/h$ or 200LFM around the CPU slot). Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 400 or 600LFM.

The table showing the supported processors above give also the maximum power consumption (TDP = Thermal Design Power) of a particular processor. Fortunately, the power consumption is by far lower when executing typical Windows or Linux tasks. The heat dissipation increases when e.g. rendering software like the Acrobat Distiller is executed.

The Core™2 Duo processors support Intel's Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in multiple steps down to 1200MHz. Furthermore they can reduce their FSB clock speed to half the frequency. This leads to an obvious reduction of power consumption resulting in less heating. This mode of lowering the processor core temperature is called TM2 (TM=Thermal Monitor).

Another way to reduce power consumption is to modulate the processor clock. This mode (TM1) is achieved by actuating the 'Stop Clock' input of the CPU. A throttling of 50% e.g. means a duty cycle of 50% on the stop clock input. However, while saving considerable power consumption, the data throughput of the processor is also reduced. The processor works at full speed until the core temperature reaches a critical value. Then the processor is throttled by 50%. As soon as the high temperature situation disappears the throttling will be disabled and the processors runs at full speed again.

A similar feature is embedded within the Graphics and Memory Controller (GMCH) GS45. An on-die temperature sensor is used to protect the GMCH from exceeding its maximum junction temperature ($T_{J,max}$=100°C) by reducing the memory bandwidth.

These features are controllable by BIOS menu entries. By default the BIOS of the CCM-BOOGIE enables mode TM2 which is the most efficient.

Main Memory

The CCM-BOOGIE features two channels of DDR3 SDRAMs. One channel is realized with 8 memory devices soldered to the board (Memory Down) and delivers a capacity of up to 4GB with a clock frequency of 1066MHz (PC3-8500).

The 2nd channel provides a socket for installing a 204-pin SODIMM module thus allowing a simple expansion of system memory (max. module height = 1.25 inch). Supported are unbuffered DDR3 SODIMMs (V_{CC}=1.5V) without ECC featuring on-die termination (ODT), according the PC3-6400 or PC3-8500 specification. Minimum module size is 256MB; maximum module size is 4GB.

Due to the video requirements of the GS45 chipset, it is recommended to add a SODIMM module with same size as the Memory Down to get best performance (some of the system memory is dedicated to the graphics controller). This typically results in a size of 2x1GB of memory which is recommended to run the operating systems Windows 2000, Windows XP or Windows Vista.

The GS45 chipset supports symmetric and asymmetric memory organization. The maximum memory performance can be obtained by using the symmetric mode. When in this mode, the GMCH accesses the memory channels in an interleaved way. Since the GS45 supports Intels Flex Memory Technology, interleaved operation isn't limited to systems using memory channels of equal capacity. In the case of unequal memory population the smaller memory channel dictates the address space of the interleaved accessible memory region. The remainder of the memory is then accessed in non-interleaved mode.

In asymmetric mode the memory always will be accessed in a non-interleaved manner with the drawback of less bandwidth. The only meaningful application of asymmetric mode is the special case when only one memory channel is populated (i.e. the SODIMM socket may be left empty).

The contents of the SPD EEPROM on the SO-DIMM is used by the BIOS at POST (Power-on Self Test) to get any necessary timing parameters to program the memory controller within the chipset.

LAN Subsystem

The Ethernet LAN subsystem is composed of two Gigabit Ethernet ports: One Intel 82567LM Physical Layer Transceiver (PHY) using the ICH9 internal MAC and one Intel 82574L Gigabit Ethernet Controller. These devices provide also legacy 10Base-T and 100Base-TX connectivity. The Ethernet ports are fed to two RJ45 jacks located in the front panel. Each port includes the following features:

- One PCI Express lane per Ethernet port (250MB/s)
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T (Classic Ethernet) capability.
- Half- or full-duplex operation.
- IEEE 802.3u, 802.3ab Auto-Negotiation for the fastest available connection.
- Jumperless configuration (complete software-configurable).
- Two bicoloured LEDs integrated into the dedicated RJ-45 connector to signal the LAN link, the LAN connection speed and activity status.

Each device is connected by a single PCI Express lane to the chipset (ICH9). Their MAC addresses (unique hardware number) are stored in dedicated FLASH/EEPROM components. The Intel Ethernet software and drivers for the 82567 and 82574 is available from Intel's World Wide Web site for download.

When managing the board by Intel Active Management Technology (iAMT), the dedicated network port to do so is accessible by the RJ45 connector GbE1.

Serial ATA Interface (SATA)

The CCM-BOOGIE provides six serial ATA (SATA) ports each capable of transferring 3Gbps (300MByte/s). Three of the four ports integrated within the ICH9 are routed to the *CompactPCI* J2 connector, thus they are accessible via the rear I/O transition module CCT-RIO. The remainder SATA channel of the ICH9 and two further ports coming from an additional controller (JMicron JMB362) are fed to the high speed expansion connector J_HSE. This connector allows the installation of local expansion boards like C40-SCFA to attach the popular CompactFlash cards.

A LED named HD located in the front panel, signals disk activity status of the SATA devices.

Available for download from Intel's and JMicron's web sites are drivers for popular operating systems, e.g. Windows® 2000, Windows® XP, Windows® Vista and Linux.

Graphics Subsystem

The graphics subsystem is part of the Intel GS45 Graphics/Memory Controller Hub (GMCH). The CCM-BOOGIE offers two digital (SDVO) and one analog (VGA) interface. One of the SDVO ports and the VGA interface is provided by a DVI-I graphics connector. This is both a digital and analog interface. Recent digital input flat-panel displays are widely available with this connector style. For classic monitors, adapters or adapter cables can be used for converting from DVI-I to the 15-pin HD D-SUB connector.

A special display transmitter chip is used to convert Intel's proprietary, PCI express based SDVO interface to the differential DVI signals. The SiI1362 (Silicon Image) transmitter uses PanelLink® Digital technology to support displays ranging from VGA to UXGA resolutions (25 - 165Mpps) in a single link interface.

The 2nd SDVO port is fed to the on-board connector J_SDVO. Expansion boards like CCO-CONCERT feature the display transmitter and provide a 2nd DVI channel via a pure digital DVI-D connector. Further more J_SDVO offers the possibility to gain access to the VESA standard interface called DisplayPort (DP) on future EKF expansion boards.

As an option, the CCM-BOOGIE can be equipped with an ordinary HD D-Sub 15-lead connector (VGA style). This connector is suitable for analog signals only, so the PanelLink transmitter is not stuffed with this option. Nevertheless also flat-panel displays can be attached to the D-Sub connector but with minor reduced image quality.

Independent from the video connector actually in use, DVI or VGA, the VESA DDC 2B standard is supported. This is a two-wire serial bus (clock, data), which is controlled by the GMCH and allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. In addition, DDC Power (+5V) is delivered to either connector. A resettable fuse is stuffed to protect the board from an external short-circuit condition (0.75A).

Graphics drivers for the GS45 can be downloaded from the Intel web site.

Real-Time Clock

The CCM-BOOGIE has a time-of-day clock and 100-year calendar, integrated into the ICH9. A battery on the board keeps the clock current when the computer is turned off. The CCM uses a BR2032 lithium battery soldered in the board, giving an autonomy of more than 5 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

Universal Serial Bus (USB)

The CCM-BOOGIE is provided with eleven USB ports, all of them are USB 2.0 capable. Two USB interfaces are routed to front panel connectors, two ports are feed to the expansion board interface connectors J_EXP, four to the high speed expansion connector J_HSE, and three ports are optionally available for rear I/O across the J2/P2 *CompactPCI* connector.

The front panel USB connectors can source up to 0.5A/5V each, over-current protected by two electronic switches. Protection for the USB ports on the expansion interfaces and on the rear I/O connector is located on expansion boards like CCO-CONCERT-MARIACHI and the CCT-RIO respective. The USB controllers are integrated into the ICH9.

LPC Super-I/O Interface

In a modern system, legacy ports as PS/2 keyboard/mouse, COM1/2 and LPT have been replaced by USB and Ethernet connectivity. The 1.4MB floppy disk drive has been swapped against CD- or DVD-RW drives, attached to a SATA connector, or USB memory sticks. Hence, the CCM-BOOGIE is virtually provided with all necessary I/O ports. However, for compatibility purposes the CCM is additionally equipped with a simple Super-I/O chip, for optional rear I/O of PS/2 keyboard/mouse and COM1 (TTL level only) across the J2/P2 CPCI connector. The Super-I/O controller resides on the local LPC bus (LPC = Low Pin Count interface standard), which is a serialized ISA bus replacement.

As an alternative, EKF offers multiple expansion boards to the CCM-BOOGIE, featuring all classic Super-I/O functionality. For example the CCO-CONCERT is a 3U Eurocard with a 4HP (single) width front panel. Access to the connectors PS/2 (mouse, keyboard), COM, USB and audio in/out is given directly from the front panel. The CCO-CONCERT connects to the CCM-BOOGIE across the connectors PEXPT or PEXPB. Usually the CCH is attached to the top of the CCM-BOOGIE. Nevertheless bottom side mounting is possible on customers request.

SPI Flash

The BIOS is stored in two flash devices with Serial Peripheral Interface (SPI). 4MByte of BIOS code, AMT firmware and user data may be stored nonvolatile in these SPI flashs (up to 16MByte of flash space is available on request).

The SPI flash contents can be reprogrammed (if suitable) by a DOS or Linux based tool. This program and the latest CCM-BOOGIE BIOS binary are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the CCM-BOOGIE may no more be operable. In this case you would possibly have to send in the board, because the flash devices are directly soldered to the PCB and cannot be changed by the user.

Reset

The CCM-BOOGIE is provided with several supervisor circuits to monitor supply rails like the CPU core voltage, 1.5V, 3.3V or 5V. This circuitry is responsible also to generate a clean power-on reset signal.

Due to lack of space within the front panel the CCM-BOOGIE does not offer a classical push button to force a manual board reset. Nevertheless it is possible to reset the board manually. The ejector within the front panel contains a micro switch that is used to generate a board reset signal. This is done by pushing the red button of the ejector until the handle unlocks without ejecting the board. Immediately after that push up the ejector back to its original position (the red button jumps up as well). Animated GIF: www.ekf.com/c/ccpu/img/reset_400.gif

The 2nd function of the red push button is to act as the board's power button. When pressing besides the reset also a power button event is created.

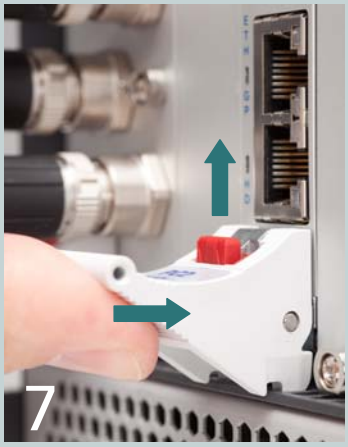
NOTE: To prevent the board to cause a power button override, the handle should be closed immediately after unlocking the front panel handle. A power button override is triggered by opening the front panel handle for at least 4 seconds. It results in bringing the board to power state S5. In case of entering this state, unlock and lock the front panel handle a 2nd time to reenter normal power state S0 again. See also section 'PG (Power Good) LED' to see how the CCM-BOOGIE indicates the different power states.

WARNING: The CCM-BOOGIE will enter the power state S5 if the front panel handle is not closed properly when the system powers up. An open handle is signalled by a yellow blinking 'PG LED'.

The manual reset and power button functionality of the front panel handle could be controlled by BIOS Setup.

An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on CompactPCI connector J2 pin C17. Pulling this signal to GND will have the same effect as to push the handle's red push button.

The healthy state of the CCM-BOOGIE is indicated by the LED PG (Power Good) located in the front panel. This bicoloured LED signals different states of the board (see section below). As soon as this LED begins to shine green all power voltages are within their specifications and the reset signal has been deasserted.



Watchdog

An important reliability feature is the watchdog function, which is programmable by software. The behaviour of the watchdog is defined within the PLD, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After alerting the WD and programming the time-out value, the related software (e.g. application program) must trigger the watchdog periodically. To simplify watchdog programming all watchdog related functions can be done by calling service requests (software SMI's).

The watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a full system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it has been put on alert, whereas it is possible to reprogram its time-out value at any time.

PG (Power Good) LED

The CCM-BOOGIE offers a LED labelled PG located within the front panel. After system reset, this LED defaults to signal different board states:

- Off Sleep state S3, S4 or S5
- Red steady Hardware failure
- Red blink Software failure
- Yellow Management state S3/M1, S4/M1 or S5/M1
- Yellow blink Front panel handle is unlocked [1)]
- Green Healthy

[1)] This feature is available from board revision 1.02.2x forward.

In the states *Off* or *Yellow* the LEDs GP and HD decode the kind of sleep state as follows:

State	Description	LED GP	LED HD
S3	Suspend to RAM	OFF	ON
S4	Suspend to Disk	ON	OFF
S5	Soft Off	ON	ON

To enter the PG LED state *Software failure* an appropriate service request by software SMI must be called. The PG LED remains in this red blinking state until the next SMI request is made. After that it falls back to its default function.

HD (Hard Disk Activity) LED

The CCM-BOOGIE offers a LED marked as HD placed within the front panel. This LED signals activity on any device attached to the SATA ports. As described above this LED may change its function dependent on the state of the LED PG.

GP (General Purpose) LED

Another more programmable bicoloured LED can be observed from the front panel. The status of the red part within the GP LED is controlled by the GPO18 output of the ICH9. Setting this pin to "1" will switch on the red LED. To turn on or off the green LED an appropriate service request (software SMI) must be made.

While the CPU card is controlled by the BIOS firmware, the GP LED is used to signal board status information. A red blinking GP LED is an indication that the BIOS code couldn't start. For details please refer to www.ekf.com/c/ccpu/ccm/firmware/biosinfo.txt.

After successful operating system boot, the GP LED is not dedicated to any particular hardware or firmware function with exception of special states of the LED PG as described above. Hence it may be freely used by customer software.

Hot Swap Detection

The *CompactPCI* specification added the signal ENUM# to the PCI bus to allow the board hot swapping. This signal is routed to the GPI3 of the ICH9. A System Management Interrupt (SMI) can be requested if ENUM# changes by insertion or removal of a board.

Note that the CCM-BOOGIE itself is not a hot swap device, because it makes no sense to remove the system controller from a *CompactPCI* system. However, it is capable to recognize the hot swap of peripheral boards and to start software that is doing any necessary system reconfiguration.

Power Supply Status (DEG#, FAL#)

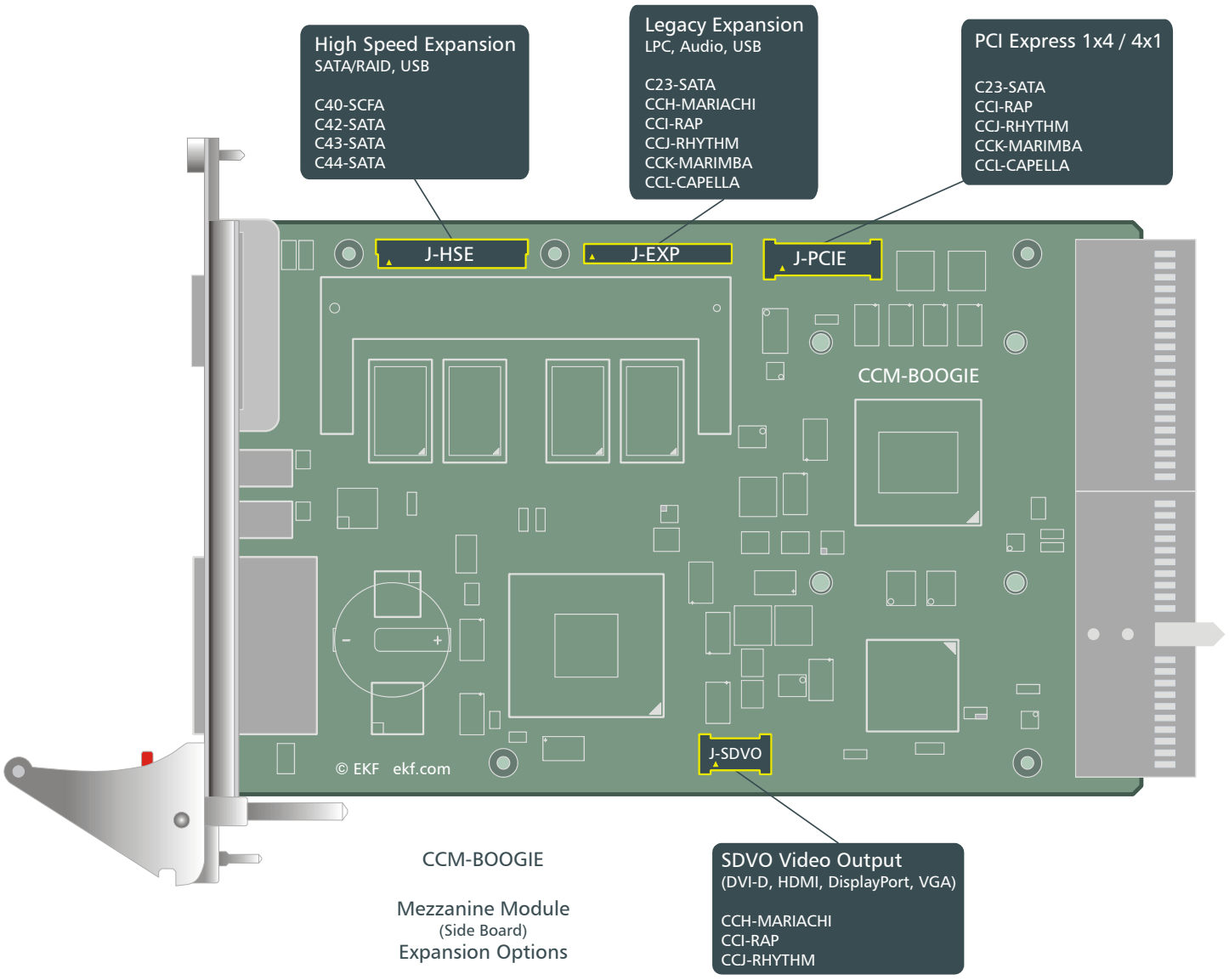
Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions of the *CompactPCI* specification and may be driven by the power supply. DEG# signals the degrading of the supply voltages, FAL# there possible failure. On the CCM-BOOGIE the signal FAL# is routed to the GPI4 and DEG# to the GPI5 of the ICH9.

PXI Trigger Signals

As an option, the CCM-BOOGIE supports four of the eight trigger signals of the PXI standard, as defined by National Instruments. The trigger signals are provided by the local SIO (Super-I/O) chip IT8761E. GPIO20/21 are routed to TRIG0/1, and GPIO26/27 are used to control TRIG6/7. These signals can also be used as GPIO lines in a non-PXI environment.

Mezzanine Side Board Options

The CCM-BOOGIE is provided with several stacking connectors for attachment of a mezzanine expansion module (aka side board), suitable for a variety of readily available mezzanine cards (please refer to www.ekf.com/c/ccpu/mezz_ovw.pdf for a more comprehensive overview). EKF furthermore offers custom specific development of side boads (please contact sales@ekf.de).

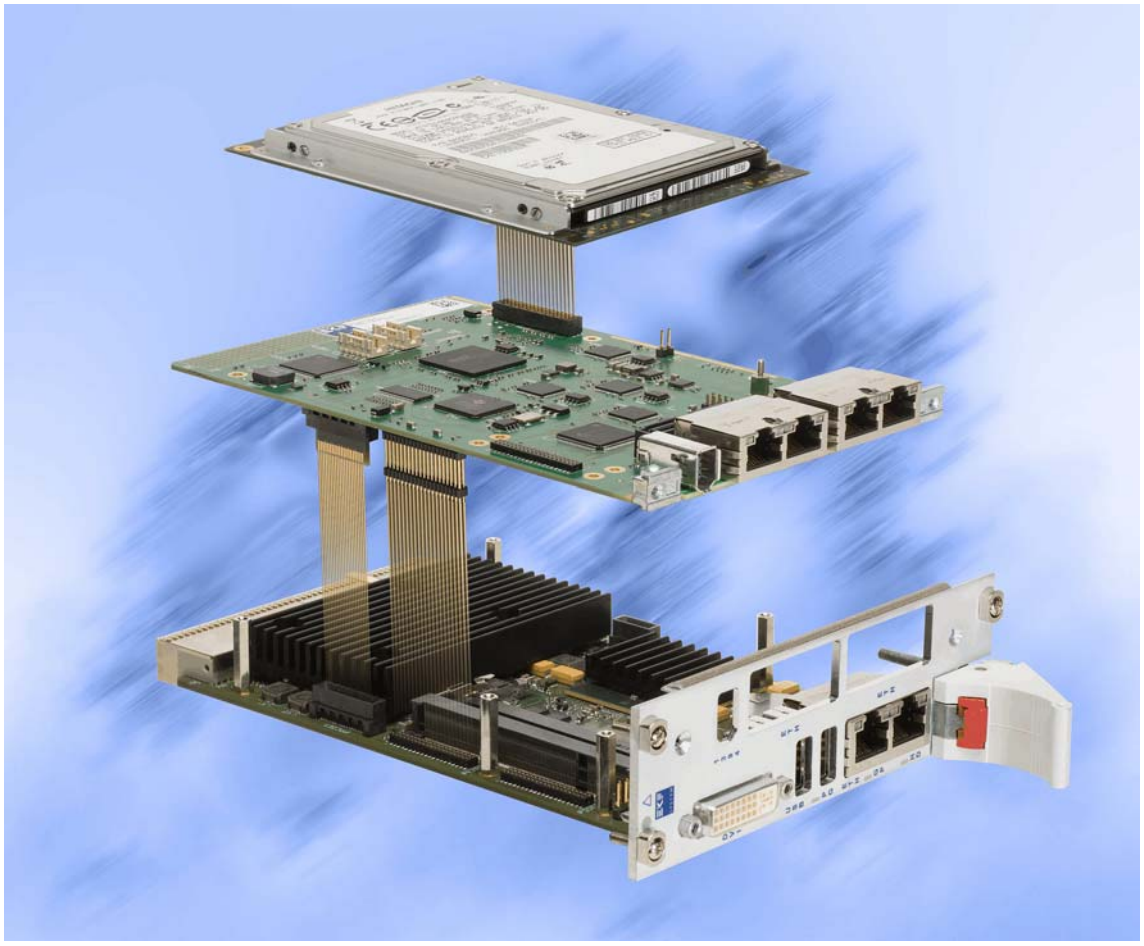


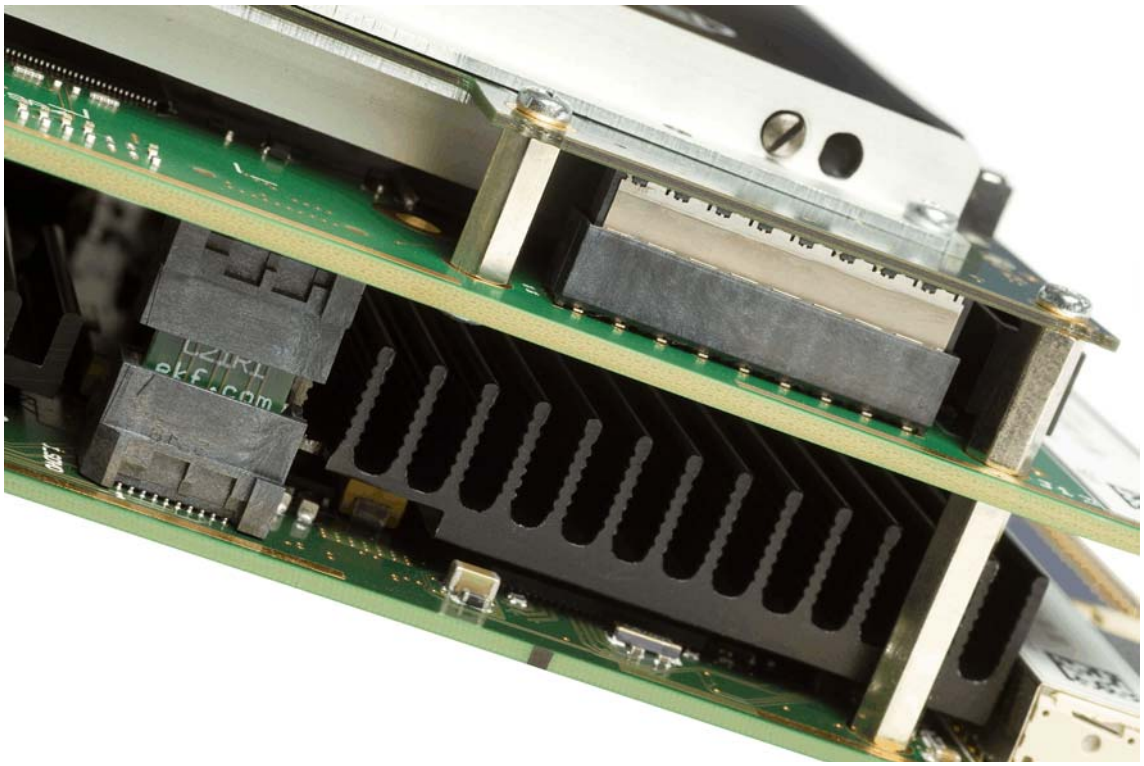
Most mezzanine expansion modules require an assembly height of 8HP in total, together with the CPU carrier board (resulting from two cards at 4HP pitch each).

In addition, cropped mezzanine modules are available for mass storage, which maintain the 4HP envelope (see illustrations next page), for extremely compact systems. Furthermore these small size modules may be combined with the full-size expansion boards (that means an assembly comprised of 3 PCBs).

Due to the SATA/USB mezzanine connector J-HSE, which replaces the P-IDE connector on previous CPU cards, parallel ATA drives on earlier side cards such as the CCJ-RHYTHM are no more supported with the CCM-BOOGIE. Please consider a low profile mezzanine module such as the C41-CFAST (CFast™ Card), C42-SATA (1.8-inch SATA SSD) or C47-MSATA (mSATA SSD module) as storage solution, mounted between the CCM-BOOGIE and the side card.

The picture below illustrates a typical mezzanine stack, comprised of the CPU carrier board (shared front panel from 4HP to 12HP, individually tailored to customers configuration), a mezzanine side board with a variety of PCIe and legacy interface functions (front panel and/or rear I/O), and a SATA storage module (either SSD or hard disk, 1.8-inch or 2.5-inch, dual or single drive, RAID option).

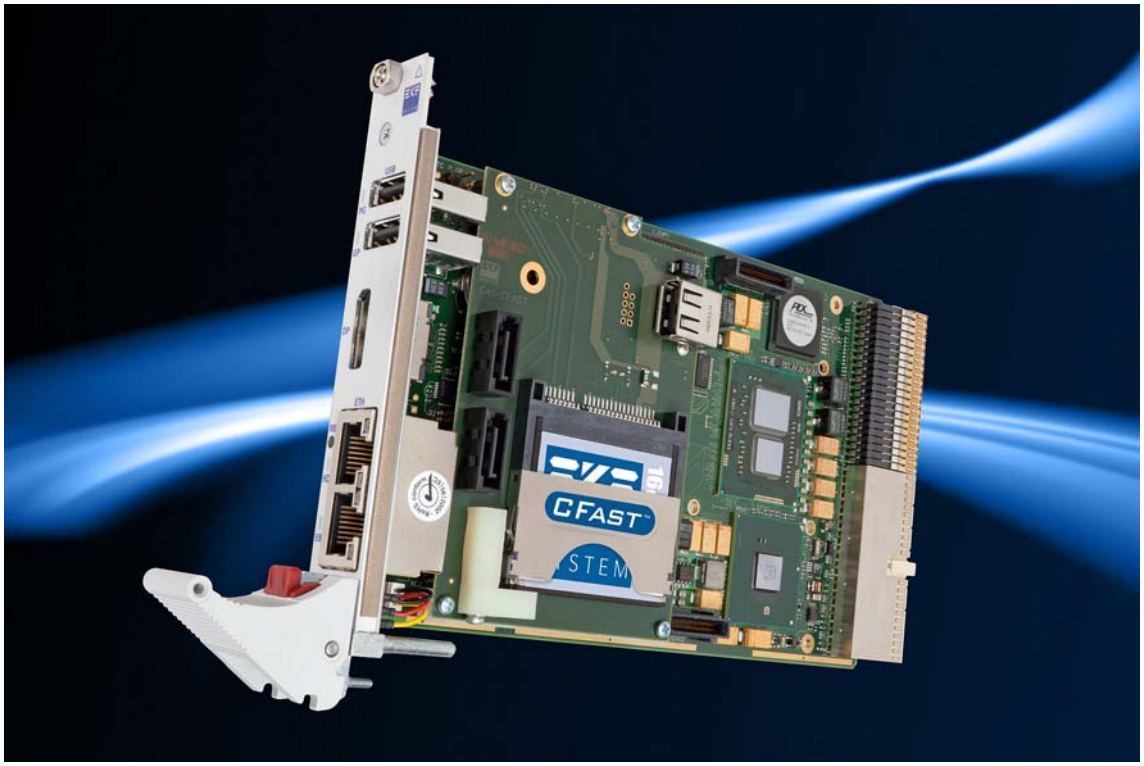




CPU Board • PMC/XMC Carrier Side Card • DX1-LYNX XMC Module (Dual Drive)

CCM-BOOGIE with C40-SCFA

C40-SCFA CompactFlash Storage Module



C41-CFAST Storage Module on CPU Carrier Card

C41-CFAST SATA Based Storage Module

CCM-BOOGIE with C42-SATA

C42-SATA Storage Module

CCM-BOOGIE with C43-SATA

C43-SATA I/O Module on CPU Carrier Card

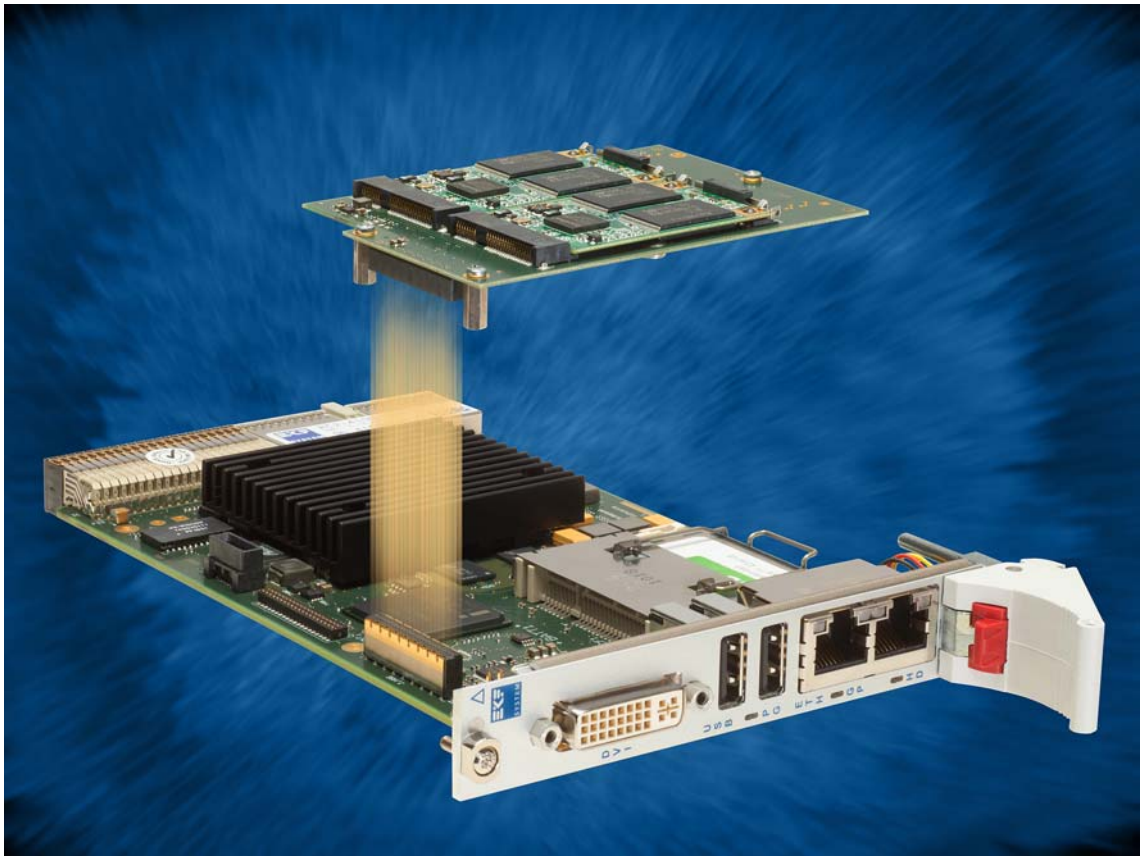
C43-SATA Mezzanine Module

CCM-BOOGIE with C44-SATA

CCM-BOOGIE w. C45-SATA (Internal Drive)

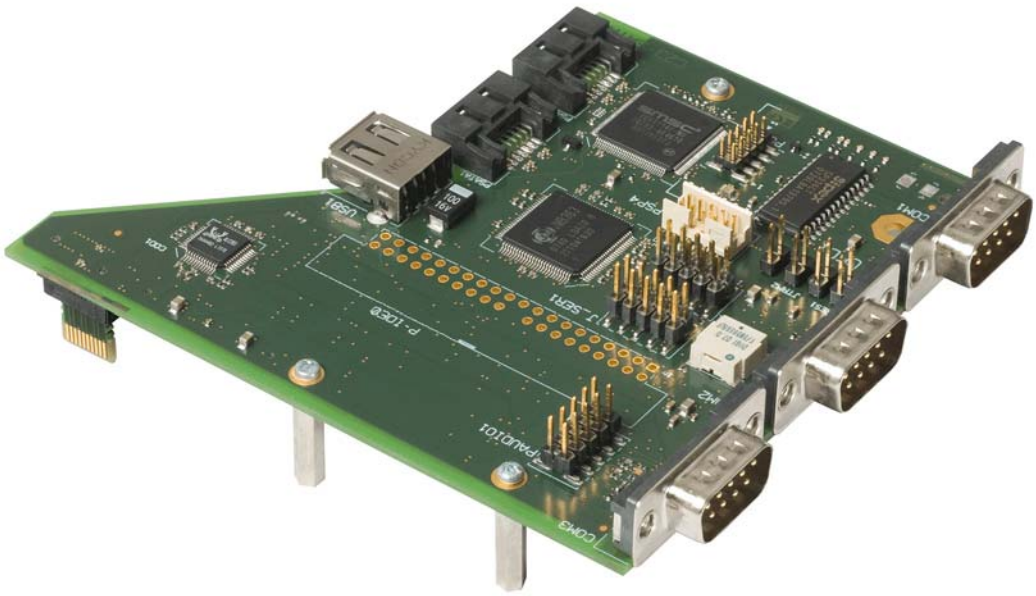
CCM-BOOGIE w. C45-SATA (Removable Drive)

C47-MSATA SSD RAID Storage Module on CPU Carrier Card



C47-MSATA over CPU Carrier Card

CCM-BOOGIE w. C23-SATA Side Board (Picture Similar)



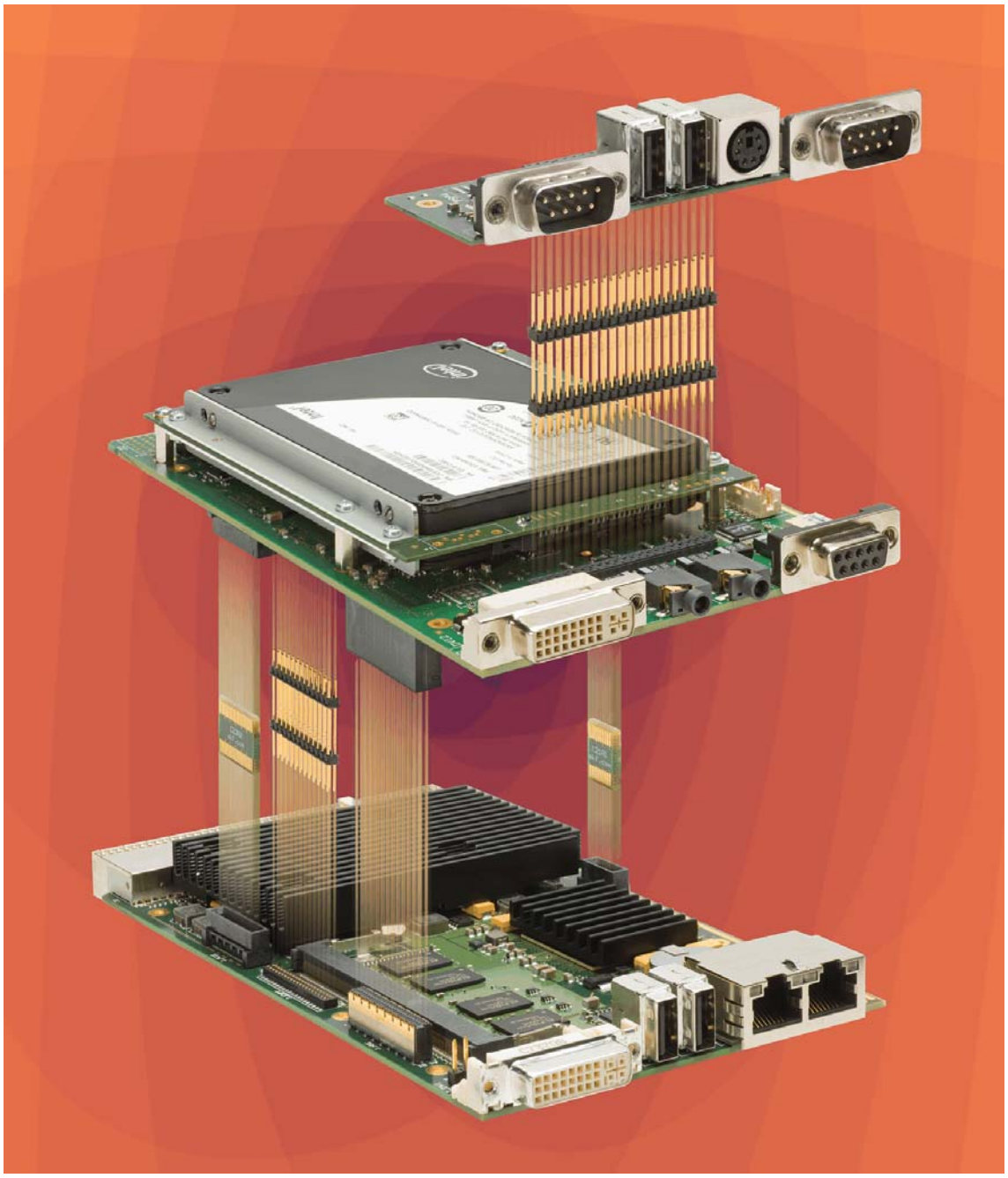
CCM-BOOGIE w. CCO-CONCERT Side Board (Similar Image)

CCM-BOOGIE w. CCI-RAP (Similar Image)

CCM-BOOGIE w. CCJ-RHYTHM Side Board (Picture Similar)

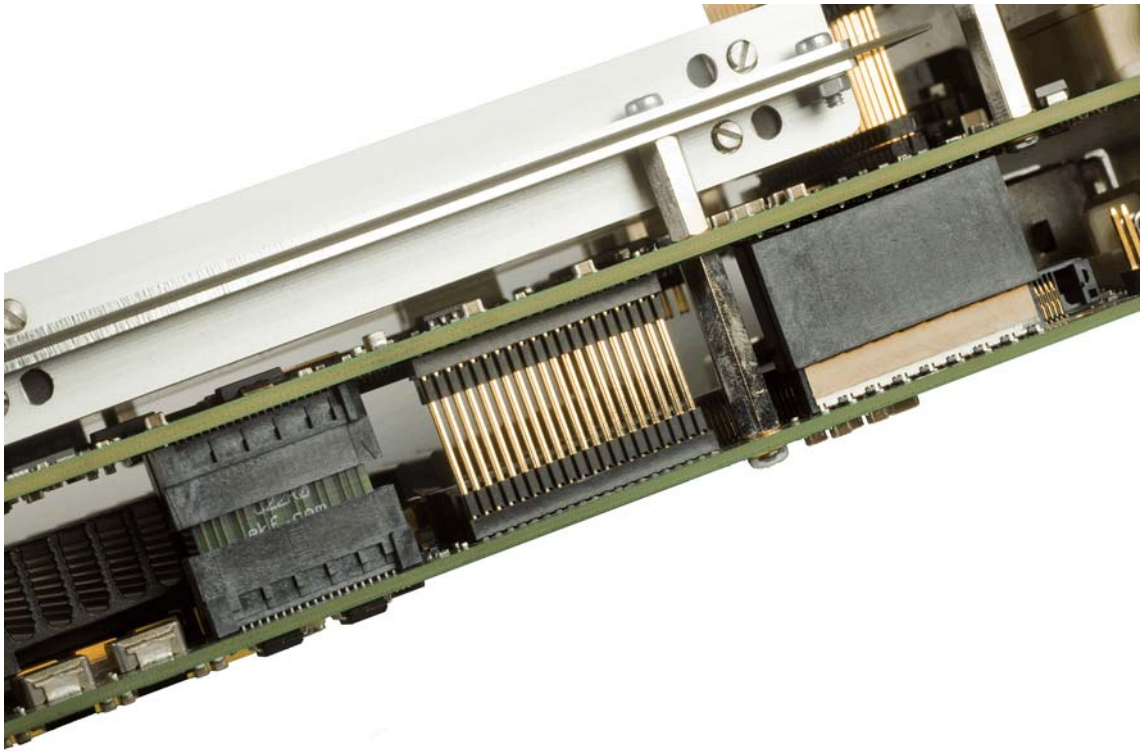
CCM-BOOGIE w. CCK-MARIMBA Side Board

CCM-BOOGIE w. CCL-CAPELLA Side Board (Similar Image)



CCM-BOOGIE w. CCO-CONCERT C20-SATA C32-FIO

CCM-BOOGIE w. CCO-CONCERT C20-SATA C32-FIO



C20-SATA

The C20-SATA is a mezzanine module, available for several side cards to the CCM-BOOGIE. The C20-SATA storage module can be equipped with one or two 2.5-inch drives (SSD or HDD).

C20-SATA Top View

C20-SATA Bottom View (Dual Drive)

Related Documents Mezzanine Modules and Side Cards	
C4x Series Mezzanine Storage Modules	www.ekf.com/c/ccpu/c4x_mezz_ovw.pdf
Mezzanine Modules Overview	www.ekf.com/c/ccpu/mezz_ovw.pdf
The EKF Mezzanine Module Concept	www.ekf.com/c/ccpu/cpci_mezzanine_evolution.pdf

Rear I/O Options

Optionally, the CCM-BOOGIE can be used for rear I/O with respect to the following functions:

- Analog Graphics
- 1 Gigabit Ethernet Port
- 3 SATA Ports
- 3 USB Ports
- Keyboard, Mouse
- COM1 (TTL Level)

The pin assignment of the rear I/O connector J2 is chosen to be plugin compatible with EKFs CPU board CCD-CALYPSO and CCG-RUMBA, thus consistent with the rear I/O module CCT-RIO.

The analog graphics and the gigabit ethernet port 1 signals are routed to multiplexers on the CCM-BOOGIE. These switches, controlled by BIOS, select either the front panel or the rear I/O connection. The COM1 port does not include the physical transceiver (TTL level only). This transceiver is located on the rear I/O module CCT-RIO instead.

The CCM is also available in versions suitable for a 64-bit *CompactPCI* backplane. However, the J2/P2 pin assignments of a 64-bit CPCI backplane differ substantially from a *CompactPCI* rear I/O backplane.

To use the rear I/O feature the system in use must be equipped with a P2 *CompactPCI* rear I/O backplane. If the system is provided with a P2 *CompactPCI* 64-bit backplane instead, several of the CCM rear I/O signals will collide with the 64-bit address/data lines on the backplane, with unpredictable results regarding the rear I/O signal integrity.

Single Slot Rear I/O Backplane EKF Part No. 932.4.01.080

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for rapair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related *CompactPCI* slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

CE

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

Installing or Replacing the Memory Module

Note: If you decide to replace the memory, observe the precautions in 'Before You Begin'

By default, the CCM-BOOGIE is delivered with onboard memory only, the SODIMM DDR3 SDRAM socket is empty.

To expand the memory a DDR3 SDRAM SODIMM module may be inserted in the socket SODM1. It is necessary to use an SODIMM that provide *Serial Presence Detect* (SPD) information, since this allows the chipset to accurately configure the memory settings for optimum performance.

A replacement memory module must match the 204-pin SODIMM form factor (known from Notebook PCs), DDR3, V_{CC}=1.5V, PC3-6400/PC3-8500 (800/1066MHz), on-die termination (ODT), unbuffered, non-ECC style. Suitable modules are available up to 4GB. The GS45 supports modules of up to a maximum of 15 address lines (A0...A14). Memory modules organized by more than 15 address lines are not suitable.

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock and to keep the values in the CMOS RAM. The battery should last during the lifetime of the CCM-BOOGIE. For replacement, the old battery must be unsoldered, and the new one soldered. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced or shorted. Replace only with the same or equivalent type. Do not expose a battery to fire.

Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. These devices consist of the Ethernet controllers and several devices within the Intel 4 series express chip set.

Bus Number	Device Number	Function Number	Vendor ID	Device ID	Description
0	0	0	0x8086	0x2A40	Host Bridge
0	2	0	0x8086	0x2A42	Internal Graphics Device
0	2	1	0x8086	0x2A43	PCI Configuration Regs.
0	3	0	0x8086	0x2A44	Management Engine 1
0	3	1	0x8086	0x2A45	Management Engine 2
0	3	2	0x8086	0x2A46	AMT IDER
0	3	3	0x8086	0x2A47	AMT SOL Redirection
0	25	0	0x8086	0x10F5	ICH9 Gigabit LAN NC1
0	26	0	0x8086	0x2937	USB UHCI Controller #4
0	26	1	0x8086	0x2938	USB UHCI Controller #5
0	26	2	0x8086	0x2939	USB UHCI Controller #6
0	26	7	0x8086	0x293C	USB 2.0 EHCI Controller #2
0	27	0	0x8086	0x293E	Intel High Definition Audio
0	28	0	0x8086	0x2940	PCI Express Port 1
0	28	1	0x8086	0x2942	PCI Express Port 2
0	28	2	0x8086	0x2944	PCI Express Port 3
0	28	3	0x8086	0x2946	PCI Express Port 4
0	28	4	0x8086	0x2948	PCI Express Port 5
0	28	5	0x8086	0x294A	PCI Express Port 6
0	29	0	0x8086	0x2934	USB UHCI Controller #1
0	29	1	0x8086	0x2935	USB UHCI Controller #2
0	29	2	0x8086	0x2936	USB UHCI Controller #3
0	29	3	0x8086	0x2939	USB UHCI Controller #6
0	29	7	0x8086	0x293A	USB 2.0 EHCI Controller #1
0	30	0	0x8086	0x2448	DMI-to-PCI Bridge
0	31	0	0x8086	0x2917	LPC Bridge

Bus Number	Device Number	Function Number	Vendor ID	Device ID	Description
0	31	2	0x8086	0x2928 0x2929 0x282A	SATA: Non-AHCI/RAID [1] SATA: AHCI Mode [1] SATA: RAID 0/1/5/10 Mode [1]
0	31	3	0x8086	0x2930	SMB Controller
0	31	5	0x8086	0x292D	SATA Controller #2
0	31	6	0x8086	0x2932	Thermal Controller
1 [2]	0	0	0x197B	0x2363	PCIe-SATA-Bridge (JMB362)
3 [2]	0	0	0x8086	0x10D3	Ethernet Controller NC2

[1] Depends on BIOS implementation.
[2] Bus number can vary depending on the PCI enumeration schema implemented in BIOS.

Local SMB Devices

The CCM-BOOGIE contains a few devices that are reachable via the System Management Bus (SMBus). These are the clock generation chip, the SPD EEPROMs for the onboard memory channel or located on the SODIMM memory module, a general purpose serial EEPROM and two supply voltage and CPU temperature controlling devices in particular. Other devices could be connected to the SMBus via the *CompactPCI* signals IPMB SCL (J1 B17) and IPMB SDA (J1 C17) or pins 29/30 of the expansion connectors J_EXPT/J_EXPB.

Address	Description
0x58	Hardware Monitor/CPU Temperature Sensor (LM87)
0x98	Processor On-Die Temerature Sensor (ADT7421)
0xA0	SPD of Onboard Memory
0xA4	SPD of SODIMM
0xAE	General Purpose EEPROM
0xD2	Main Clock Generation (CK-505)

Hardware Monitor LM87

Located on the SMBus the CCM-BOOGIE offers a hardware monitor of type LM87/NSC. This device is capable to observe board and onboard memory temperatures as well as several supply voltages generated on the board with a resolution of 8 bit. The following table shows the mapping of the voltage inputs of the LM87 to the corresponding supply voltages of the CCM-BOOGIE:

Input	Source	Resolution [mV]	Register
AIN1	CPU Core Voltage	9.8	0x28
AIN2	+1.05V	9.8	0x29
VCCP1	+1.5V	14.1	0x21
VCCP2/D2-	+1.8V	14.1	0x25
+2.5V/D2+	+0.75V	13	0x20
+3.3V	+3.3V	17.2	0x22
+5V	+5V	26	0x23
+12V	+10V	62.5	0x24

Beside the continuous measuring of temperatures and voltages the LM87 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value, the LM87 may request an interrupt via the GPI[8] of the ICH9.

GPIO Usage

GPIO Usage ICH9

CCM-BOOGIE GPIO Usage ICH9				
GPIO	Type	Tol.	Function	Description
GPIO 0	I/O	3.3V	PMSYNC#	Multiplexed with chipset internal function
GPIO 1	I	3.3V	EXP_SMI#	Expansion Interface SMI Request (J_EXP Pin 15)
GPIO 2	I	5V	CPCI_INTP	CompactPCI Interrupt Request Line INTP
GPIO 3	I	5V	CPCI_ENUM#	CompactPCI System Enumeration Line ENUM#
GPIO 4	I	5V	CPCI_FAL#	CompactPCI Power Failure Line FAL#
GPIO 5	I	5V	CPCI_DEG#	CompactPCI Power Degeneration Line DEG#
GPIO 6	O	3.3V	CPCI_INTS_EN	Connect SERIRQ to CompactPCI Line INTS LOW: SERIRQ disconnected from INTS HIGH: SERIRQ connected to INTS
GPIO 7	I	3.3V	CPCI_SYSEN#	Sense CompactPCI System Slot Enable Line SYSEN#
GPIO 8	I	3.3V	HM_INT#	Hardware Monitor LM87 Interrupt Line
GPIO 9	I/O	3.3V	N/A	Not used on CCM (fixed via resistor to GND)
GPIO 10	I	3.3V	N/A	Not used on CCM (fixed via resistor to +3.3V)
GPIO 11	I	3.3V	GP_JUMP#	BIOS CMOS Values Reset Jumper P_GP
GPIO 12	I	3.3V	N/A	Not used on CCM (fixed via resistor to GND)
GPIO 13	I	3.3V	N/A	Not used on CCM (fixed via resistor to GND)
GPIO 14	I	3.3V	N/A	Not used on CCM (fixed via resistor to +3.3V)
GPIO 15	O	3.3V	STP_PCI#	Fixed to chipset internal function
GPIO 16	O	3.3V	DPRSLPVR	Multiplexed with chipset internal function
GPIO 17	O	3.3V	CPCI_CLKEN	Enable CompactPCI Clock Buffer
GPIO 18	O	3.3V	GP_LED_RED	General Purpose LED Control (via PLD)
GPIO 19	O	3.3V	PLD_SCL	Local Option Reg Interface (within PLD)
GPIO 20	O	3.3V	SE_SYS_WP	General Purpose Serial EEPROM Write Protection
GPIO 21	O	3.3V	PLD_SDA	Local Option Reg Interface (within PLD)
GPIO 22	I	3.3V	HWREV2	PCB Revision Code Bit 2 (see GPIO 34)
GPIO 23	I	3.3V	LPC_DRQEXP#	Expansion Interface LPC DMA Request Line
GPIO 24	O	3.3V	CPCI_SMB_EN	Connect SMBus of CPCI IPMB/J_EXP to local SMBus LOW: IPMB/J_EXP disconnected from SMBus HIGH: IPMB/J_EXP connected to SMBus
GPIO 25	O	3.3V	STP_CPU#	Fixed to chipset internal function
GPIO 26	O	3.3V	N/A	Multiplexed to chipset internal function
GPIO 27	O	3.3V	VGA_SWITCH	VGA Switching Line: LOW: VGA via Rear I/O HIGH: VGA via Front I/O

CCM-BOOGIE GPIO Usage ICH9				
GPIO	Type	Tol.	Function	Description
GPIO 28	O	3.3V	ETH_SWITCH	Ethernet Switching Line: LOW: Ethernet Port #1 via Rear I/O HIGH: Ethernet Port #1 via Front I/O
GPIO 29	I	3.3V	CPCI_12VOK	CompactPCI +12V Present
GPIO 30	I	3.3V	USB_OC6#	USB Port #6 Overcurrent Detect Line
GPIO 31	I	3.3V	USB_OC7#	USB Port #7 Overcurrent Detect Line
GPIO 32	I/O	3.3V	CLKRUN#	Fixed to chipset internal function
GPIO 33	O	3.3V	NC2_EN	Enable Ethernet Controller NC2
GPIO 34	I	3.3V	HWREV0	PCB Revision Code Bit 0: GPIO 22/48/34: 000 001 010 ... 100 ... 111 Revision: 0 1 2 4 7
GPIO 35	OD	3.3V	SATACLKREQ#	Multiplexed to chipset internal function
GPIO 36-39	I	3.3V	BOARD_CFG	Board Configuration Jumpers
GPIO 40	I	3.3V	USB_OC2#	USB Front Panel Lower Port Overcurrent Detect
GPIO 41	I	3.3V	USB_J2_OC#	USB Rear I/O Port #1 or #2 Overcurrent Detect
GPIO 42	I	3.3V	USB_J2_OC#	USB Rear I/O Port #1 or #2 Overcurrent Detect
GPIO 43	I	3.3V	N/A	Not used on CCM (fixed via resistor to +3.3V)
GPIO 44	I	3.3V	USB_HSE_OC3#	USB High Speed Expansion J_HSE Port #3 Overcurrent Detect
GPIO 45	I	3.3V	USB_HSE_OC4#	USB J_HSE Port #4 Overcurrent Detect
GPIO 46	I	3.3V	USB_EXP_OC#	USB J_EXP Port #1 or #2 Overcurrent Detect
GPIO 47	I	3.3V	USB_EXP_OC#	USB J_EXP Port #1 or #2 Overcurrent Detect
GPIO 48	I	3.3V	HWREV1	PCB Revision Code Bit 1 (see GPIO 34)
GPIO 49	O	3.3V	N/A	Not used on CCM
GPIO 50	I	5V	CPCI_REQ1#	CompactPCI Bus Request Line CPCI_REQ1#
GPIO 51	O	3.3V	CPCI_GNT1#	CompactPCI Bus Grant Line CPCI_GNT1#
GPIO 52	I	5V	CPCI_REQ2#	CompactPCI Bus Request Line CPCI_REQ2#
GPIO 53	O	3.3V	CPCI_GNT2#	CompactPCI Bus Grant Line CPCI_GNT2#
GPIO 54	I	5V	CPCI_REQ3#	CompactPCI Bus Request Line CPCI_REQ3#
GPIO 55	O	3.3V	CPCI_GNT3#	CompactPCI Bus Grant Line CPCI_GNT3#
GPIO 56	I	3.3V	WDOGRST	Last Hardware Reset caused by watchdog
GPIO 57	I	3.3V	N/A	Not used on CCM (fixed via resistor to GND)
GPIO 58	O	3.3V	SPI_CS1#	Multiplexed to chipset internal function
GPIO 59	I	3.3V	USB_OC1#	USB Front Panel Upper Port Overcurrent Detect
GPIO 60	O	3.3V	N/A	Not used on CCM (fixed via resistor to +3.3V)

GPIO Usage SIO

CCM-BOOGIE GPIO Usage SIO				
GPIO	Type	Tol.	Function	Description
GPIO 13	I	5V [1)]	CPCI_64EN#	Sense CompactPCI 64-Bit Backplane (J2 Pin B5)
GPIO 14/15	I/O	5V/8mA [1)]	N/A	Not used on CCM
GPIO 16/17	I/O	5V/24mA [1)]	N/A	Not used on CCM
GPIO 20	I/O	5V/8mA [1)]	PXI_TRIG0	PXI Trigger 0 on CompactPCI J2 Pin B16
GPIO 21	I/O	5V/8mA [1)]	PXI_TRIG1	PXI Trigger 1 on CompactPCI J2 Pin A16
GPIO 22-25	I/O	5V/24mA [1)]	N/A	Not used on CCM
GPIO 26	I/O	5V/24mA [1)]	PXI_TRIG6	PXI Trigger 6 on CompactPCI J2 Pin E18
GPIO 27	I/O	5V/24mA [1)]	PXI_TRIG7	PXI Trigger 7 on CompactPCI J2 Pin E16

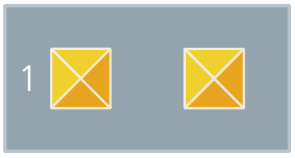
[1)] These GPIOs have pullup resistors of approx. 50kΩ within the SIO.

Configuration Jumpers

Reset Jumper BIOS CMOS RAM Values (P_GP)

The jumper P_GP is used to bring the contents of the battery backed CMOS RAM to a default state. The BIOS uses the CMOS to store configuration values, e.g. the actual boot devices. Using this jumper is only necessary, if it is not possible to enter the setup of the BIOS. To reset the CMOS RAM mount a jumper on P_GP and perform a system reset. As long as the jumper is stuffed the BIOS will use the default CMOS values after any system reset. To get normal operation again, the jumper has to be removed.

P_GP



1=GPI 2=GND

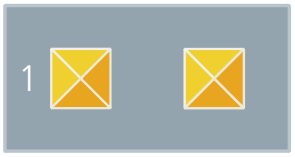
P_GP	Function
Jumper OFF [1)]	No CMOS reset performed
Jumper ON	CMOS reset performed

[1)] This setting is the factory default.

Reset Jumper ICH9 RTC Core (P_RTC)

The jumper P_RTC is used to reset the battery backed core of the ICH9. This effects some registers within the ICH9 RTC core that are important before the CPU starts its work after a system reset. Note that P_RTC will neither perform the clearing of the CMOS RAM values nor resets the real time clock. To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of P_RTC for about 1 sec. After that reinstall the board to the system and switch on the power. It is important to accomplish the RTC reset while the board has no power.

P_RTC



1=RTCRST# 2=GND

P_RTC	Function
Jumper OFF [1)]	No RTC reset performed
Jumper ON	RTC reset performed

[1)] This setting is the factory default.

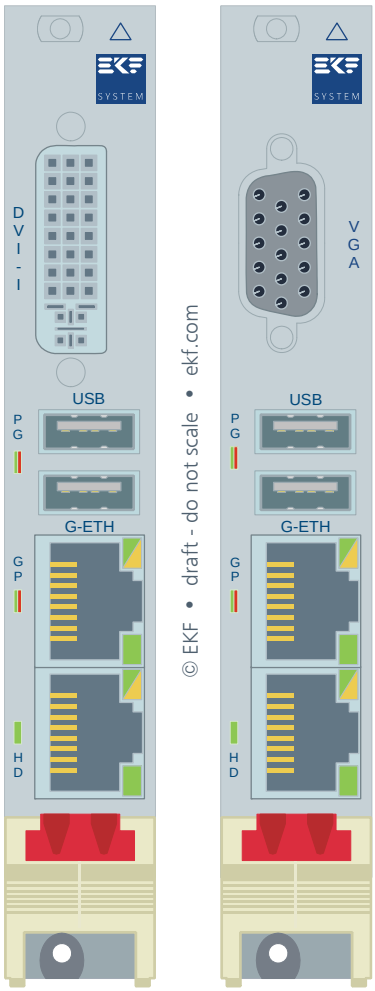
Connectors

Caution

Some of the internal connectors provide operating voltage (3.3V and 5V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are overcurrent protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel Connectors

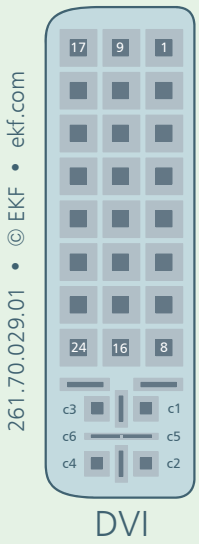
Typical CCM-BOOGIE Front Panel Elements



CCM-BOOGIE DVI

CCM-BOOGIE VGA

Video Monitor Connector J_DVI



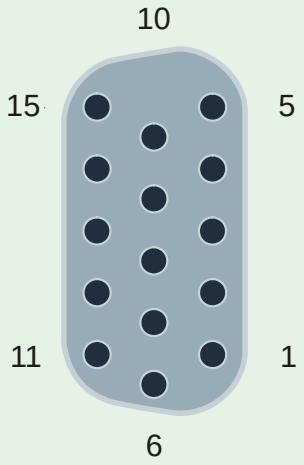
J_DVI											
17	TX0-	9	TX1-	1	TX2-						
18	TX0+	10	TX1+	2	TX2+						
19	GND	11	GND	3	GND						
20		12		4							
21		13		5							
22	GND	14	DDC_POW [1]	6	DVI_DDC_SCL						
23	TXC+	15	GND	7	DVI_DDC_SDA						
24	TXC-	16	DVI_HP	8	VSYNC [2]						
	c3	BLUE [2]	c1	RED [2]							
	c6	GND	c5	GND							
	c4	HSYNC [2]	c2	GREEN [2]							

1) +5V protoected by a PolySwitch Fuse 0.75A.
2) This signal may be switched either to the front connector or to the rear I/O adapter CCT-RIO.

For attachment of an ordinary analog RGB monitor to the J_DVI receptacle, there are both adapters and also adapter cables available from J_DVI to the HD-SUB15 connector. Attachment of digital monitors (flat panel displays) should be done by means of a DVI to DVI cable (single link style cable is sufficient).

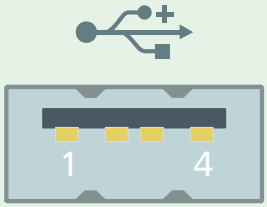
Video Monitor Connector J_VGA

As an option, the CCM-BOOGIE can be equipped with a legacy VGA connector (High-Density D-Sub 15-position female connector). The connector J_VGA replaces the J_DVI receptacle, and the digital video interface therefore is not available with this option.

J_VGA (Option)		
	1	RED [2]
	2	GREEN [2]
	3	BLUE [2]
	4	NC
	5	GND
	6	GND
	7	GND
	8	GND
	9	DDC_POW [1]
	10	GND
	11	NC
	12	VGA_DDC_SDA [2]
	13	HSYNC [2]
	14	VSYNC [2]
	15	VGA_DDC_SCL [2]

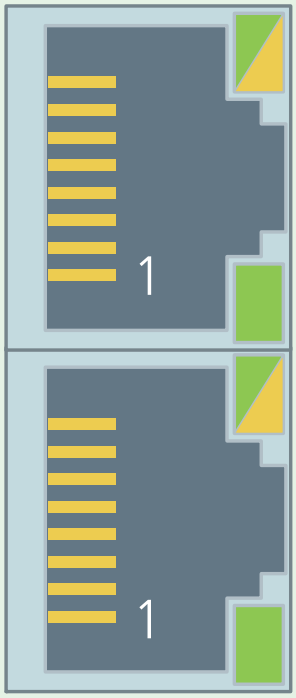
[1] +5V protoected by a PolySwitch Fuse 0.75A
[2] This signal may be switched either to the front connector or to the rear I/O adapter CCT-RIO.

USB Connectors

USB Ports 1/2 (J_USB1/J_USB2)		
 USB Receptacle © EKF • ekf.com 270.20.04.1	1	POW [1)]
	2	USB DATA NEG
	3	USB DATA POS
	4	GND

1) +5V protected by an Electronic Fuse 0.5A

Ethernet Connectors

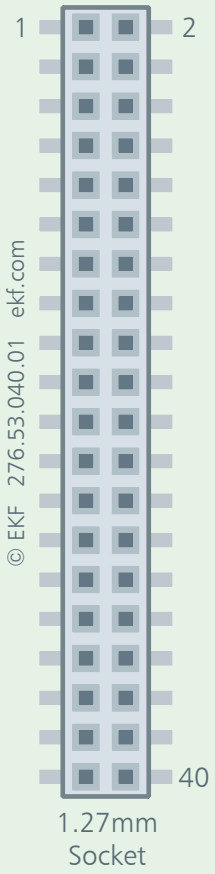
G-ETH1/2 (RJ45)		
 270.02.08.5	1	NC1_MDX0+ [1]
	2	NC1_MDX0- [1]
	3	NC1_MDX1+ [1]
	4	NC1_MDX2+ [1]
	5	NC1_MDX2- [1]
	6	NC1_MDX1- [1]
	7	NC1_MDX3+ [1]
	8	NC1_MDX3- [1]
	1	NC2_MDX0+
	2	NC2_MDX0-
	3	NC2_MDX1+
	4	NC2_MDX2+
	5	NC2_MDX2-
	6	NC2_MDX1-
	7	NC2_MDX3+
	8	NC2_MDX3-

[1] This signal may be switched either to the front connector or to the rear I/O adapter CCT-RIO.

The upper green/yellow dual-LED signals 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off. The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established.

Internal Connectors

Expansion Interface Header J_EXP



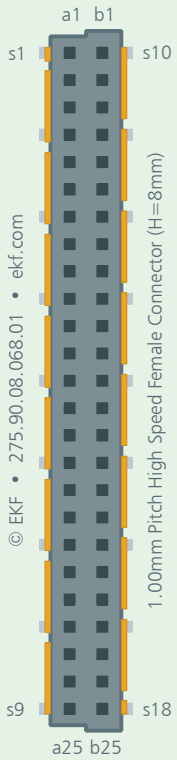
J_EXPT (J_EXPB optinal)			
GND	1	2	+3.3V [1]
PCI_CLK	3	4	PLTRST#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRM#	9	10	LPC_DRQ#
GND	11	12	+3.3V [1]
SERIRQ	13	14	EXP_PME#
EXP_SMI#	15	16	SIO_CLK14
FWH_ID0	17	18	FWH_INIT#
ICH_RCIN#	19	20	ICH_A20GATE
GND	21	22	+5V [1]
USB_EXP_P2-	23	24	USB_EXP_P1-
USB_EXP_P2+	25	26	USB_EXP_P1+
USB_EXP_OC#	27	28	H_DBRESET#
EXP_SCL [2]	29	30	EXP_SDA [2]
GND	31	32	+5V [1]
HDA_SDOUT	33	34	HDA_SDIN0
HDA_RST#/CL_RST# [3]	35	36	HDA_SYNC
HDA_BITCLK/CL_CLK [3]	37	38	HDA_SDIN1/CL_DATA [3]
SPEAKER	39	40	+12V [4]

[1] Power rail switched on in state S0 only.
[2] Connected to SMBus via switch, isolated after PCI reset.
[3] Stuffing option, default is the HDA option.
[4] Unswitched power rail (switched on always).

The expansion interface header footprint is available on both sides of the board, top and bottom. Nevertheless the bottom side connector is stuffed only on customers request.

WARNING: Neither the +3.3V pin, nor the +5V pin, nor the +12V pin are protected against a short circuit situation! This connector therefore should be used only for attachment of an expansion board. The maximum current flowing across these pins should be limited to 2A per power rail.

High Speed Expansion Connector J_HSE



High Speed Expansion J_HSE			
GND	a1	b1	GND
SATA_HSE1_TXP [3) 6)]	a2	b2	SATA_HSE3_TXP [4) 6)]
SATA_HSE1_TXN [3) 6)]	a3	b3	SATA_HSE3_TXN [4) 6)]
GND	a4	b4	GND
SATA_HSE1_RXN [3) 6)]	a5	b5	SATA_HSE3_RXN [4) 6)]
SATA_HSE1_RXP [3) 6)]	a6	b6	SATA_HSE3_RXP [4) 6)]
GND	a7	b7	GND
SATA_HSE2_TXP [4) 6)]	a8	b8	*SATA_HSE4_TXP* [5) 6)]
SATA_HSE2_TXN [4) 6)]	a9	b9	*SATA_HSE4_TXN* [5) 6)]
GND	a10	b10	GND
SATA_HSE2_RXN [4) 6)]	a11	b11	*SATA_HSE4_RXN* [5) 6)]
SATA_HSE2_RXP [4) 6)]	a12	b12	*SATA_HSE4_RXP* [5) 6)]
GND	a13	b13	GND
USB_HSE1_P	a14	b14	USB_HSE3_P
USB_HSE1_N	a15	b15	USB_HSE3_N
GND	a16	b16	GND
USB_HSE2_P	a17	b17	USB_HSE4_P
USB_HSE2_N	a18	b18	USB_HSE4_N
GND	a19	b19	GND
USB_HSE1_OC#	a20	b20	USB_HSE3_OC#
USB_HSE2_OC#	a21	b21	USB_HSE4_OC4
+3.3VS [1)]	a22	b22	+5VS [1)]
+3.3VS [1)]	a23	b23	+5VS [1)]
+3.3VA [2)]	a24	b24	+5VA [2)]
+12VA [2)]	a25	b25	*RSVD*

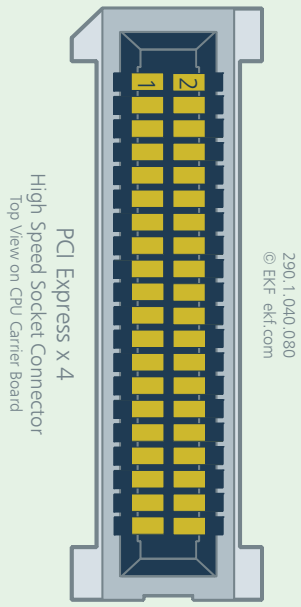
1) Power rail switched on in state S0 only.
2) Power rail switched on with system power.
3) This SATA channel has been derived from ICH9.
4) These SATA channels are derived from the JMB362.
5) For future use, not connected on CCM-BOOGIE.
6) All TX/RX designations with respect to SATA controller.

WARNING: Neither the +3.3V pins, nor the +5V pins, nor the +12VA pin are protected against a short circuit situation! This connector therefore should be used only for attachment of the C40-SCFA adapter or an expansion board. The maximum current flowing across these pins should be limited to 2A per power rail.

Mounting Area for Low Profile Mezzanine Storage Modules

Sample J_HSE Based Low Profile Mezzanine Module

PCI Express Expansion Header J_PCIE

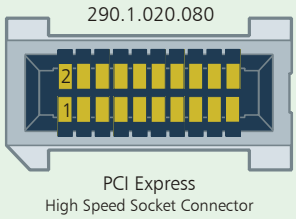


J_PCIE			
GND	1	2	GND
+5V [1]	3	4	+3.3V [1]
+5V [1]	5	6	+3.3V [1]
GND	7	8	GND
PE_CLKP	9	10	PLTRST#
PE_CLKN	11	12	PE_WAKE#
GND	13	14	GND
PE_1TP	15	16	PE_1RP
PE_1TN	17	18	PE_1RN
GND	19	20	GND
GND	21	22	GND
PE_2TP	23	24	PE_2RP
PE_2TN	25	26	PE_2RN
GND	27	28	GND
PE_3TP	29	30	PE_3RP
PE_3TN	31	32	PE_3RN
GND	33	34	GND
PE_4TP	35	36	PE_4RP
PE_4TN	37	38	PE_4RN
GND	39	40	GND

[1] Power rail switched on in state S0 only.

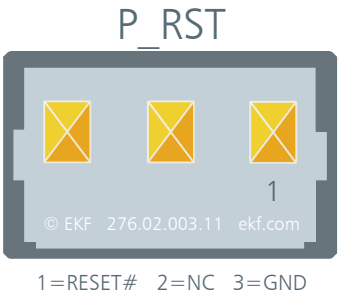
WARNING: Neither the +3.3V pin, nor the +5V pin are protected against a short circuit situation! The maximum current flowing across these pins should be limited to 2A per power rail.

SDVO Expansion Header J_SDVO

J_SDVO				
	GND	1	2	GND
	SDVO_RED+	3	4	SDVO_CLK+
	SDVO_RED-	5	6	SDVO_CLK-
	GND	7	8	GND
	SDVO_GREEN+	9	10	SDVO_INT+
	SDVO_GREEN-	11	12	SDVO_INT-
	GND	13	14	GND
	SDVO_BLUE+	15	16	SDVO_CTR_CLK
	SDVO_BLUE-	17	18	SDVO_CTR_DATA
	GND	19	20	GND

System Reset Header P_RST

The jumper P_RST is used to perform a manually system reset. By default P_RST is connected with a short cable to a micro switch located within the front panel handle. The switch performs a system reset by short-circuiting the pins 1 and 3 of P_RST.



PLD Programming Header P_ISP

Note: P_ISP is not stuffed. Its footprint is situated at the bottom side of the board.

Processor Debug Header XDP1

XDP1			
1	PREQ#/BPM5#	BCLKN/HOOK5	13
2	PRDY#/BPM4#	VCC	14
3	GND	RST#/HOOK6	15
4	BPM3#	DBR#/HOOK7	16
5	BPM2#	GND	17
6	GND	TDO	18
7	BPM1#	TRST#	19
8	BPM0#	TDI	20
9	GND	TMS	21
10	PWRGD/HOOK0	TCK1 (NC)	22
11	HOOK2 (NC)	GND	23
12	BCLKP/HOOK4	TCK0	24

Note: XDP1 is not stuffed. Its footprint is situated at the bottom side of the board.

CompactPCI J1

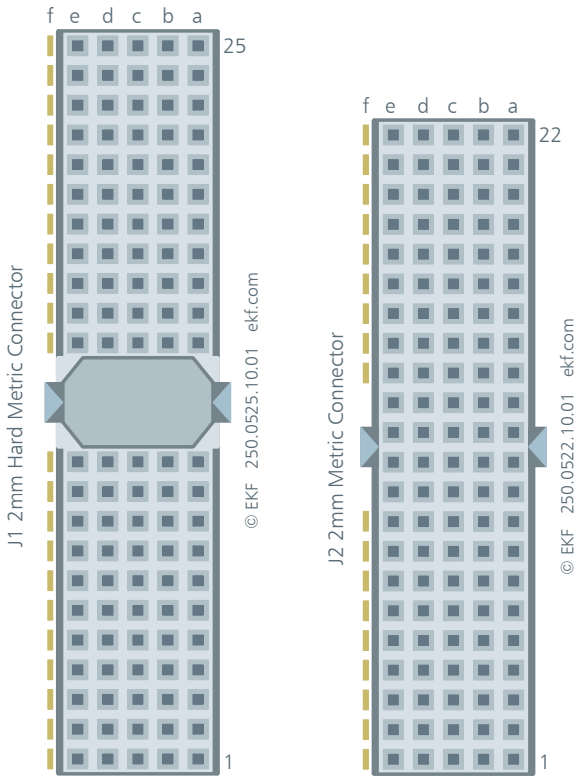
J1	A	B	C	D	E
25	5V	*REQ64#* [2]	ENUM# [1]	3.3V	5V
24	AD1	5V	V(I/O)	AD0	*ACK64#* [2]
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	M66EN [3]	C/BE0#
20	AD12	GND	V(I/O)	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR# [1]	GND	3.3V	PAR	C/BE1#
17	3.3V	IPMB SCL [4]	IPMB SDA [4]	GND	PERR# [1]
16	DEVSEL# [1]	GND	V(I/O)	STOP# [1]	LOCK# [1]
15	3.3V	FRAME# [1]	IRDY# [1]	*GND/BD_SEL#* [5]	TRDY# [1]
14	KEY AREA				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	GND	AD23	GND	AD22
8	AD26	GND	V(I/O)	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ# [1]	GND	3.3V	CLK	AD31
5	*BRSVP1A5* [5]	*BRSVP1B5* [5]	RST#	GND	GNT#
4	IPMB PWR	GND	V(I/O)	INTP [1]	INTS [1]
3	INTA# [1]	INTB# [1]	INTC# [1]	5V	INTD# [1]
2	*TCK* [5]	5V	*TMS* [5]	*TDO* [5]	*TDI* [5]
1	5V	-12V [6]	*TRST#* [5]	+12V	5V

[1] This pin is pulled up with 1kΩ to V(I/O). Other pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.
[2] This pin is not used on CCM-BOOGIE, but pulled up with 1kΩ to V(I/O). Other pull up resistor values on request.
[3] This pin is fixed to GND on CCM-BOOGIE to force 33MHz operation since 66MHz operation is not supported.
[4] This pin is pulled up with 3.0k to J1 pin A4.
[5] This pin is not connected.
[6] This pin is not used on CCM-BOOGIE.

CompactPCI J2

J2	A	B	C	D	E
22	*GA4* [5]	*GA3* [5]	*GA2* [5]	*GA1* [5]	*GA0* [5]
21	CLK6	GND	*RSV* NC1_MX2-	*RSV* NC1_MX3-	*RSV* NC1_MX3+
20	CLK5	GND	*RSV* NC1_MX2+	GND	*RSV* NC1_MX0+
19	GND	GND	*RSV* NC1_MX1-	*RSV* NC1_MX1+	*RSV* NC1_MX0-
18	*BRSVP2A18* VGA_RED	*BRSVP2B18* VGA_GREEN	*BRSVP2C18* VGA_HSYNC	GND	*BRSVP2E18* PXI_TRIG6 [3] VGA_VSYNC
17	*BRSVP2A17* VGA_BLUE	GND	PRST# [1]	REQ6# [1]	GNT6#
16	*BRSVP2A16* PXI_TRIG1 [3]	*BRSVP2B16* PXI_TRIG0 [3] DDC_SCL [2]	DEG# [1]	GND	*BRSVP2E16* PXI_TRIG7 [3] DDC_SDA [2]
15	*BRSVP2A15*	GND	FAL# [1]	REQ5# [1]	GNT5#
14	*AD35* [1] SATA_2RN	*AD34* [1] SATA_2RP	*AD33* [1] SATA_ACT#	GND	*AD32* [1] GND
13	*AD38* [1] GND	GND	V(I/O)	*AD37* [1] SATA_2TP	*AD36* [1] SATA_2TN
12	*AD42* [1] SATA_1RN	*AD41* [1] SATA_1RP	*AD40* [1]	GND	*AD39* [1] GND
11	*AD45* [1] GND	GND	V(I/O)	*AD44* [1] SATA_1TP	*AD43* [1] SATA_1TN
10	*AD49* [1] SATA_0RN	*AD48* [1] SATA_0RP	*AD47* [1]	GND	*AD46* [1] GND
9	*AD52* [1] GND	GND	V(I/O)	*AD51* [1] USB_P4P	*AD50* [1] USB_P4N
8	*AD56* [1] SATA_0TN	*AD55* [1] SATA_0TP	*AD54* [1] GND	GND COM1_DSR#	*AD53* [1] COM1_TXD
7	*AD59* [1] COM1_DTR#	GND COM1_CTS#	V(I/O) COM1_RXD	*AD58* [1] COM1_RTS#	*AD57* [1] COM1_DCD#
6	*AD63* [1] USB_P2P	*AD62* [1] USB_P2N	*AD61* [1] USB_P3P	GND USB_OC34#	*AD60* [1] USB_P3N
5	*C/BE5#* [1] +5V/1.5A [4]	64EN# [1]	V(I/O)	*C/BE4#* [1] MS_DATA	*PAR64* [1] MS_CLK
4	V(I/O)	*BRSVP2B4* [6] +5V/1.5A [4]	*C/BE7#* [1] KB_DATA	GND	*C/BE6#* [1] KB_CLK
3	CLK4	GND	GNT3#	REQ4# [1]	GNT4#
2	CLK2	CLK3	SYSEN# [7]	GNT2#	REQ3# [1]
1	CLK1	GND	REQ1# [1]	GNT1#	REQ2# [1]

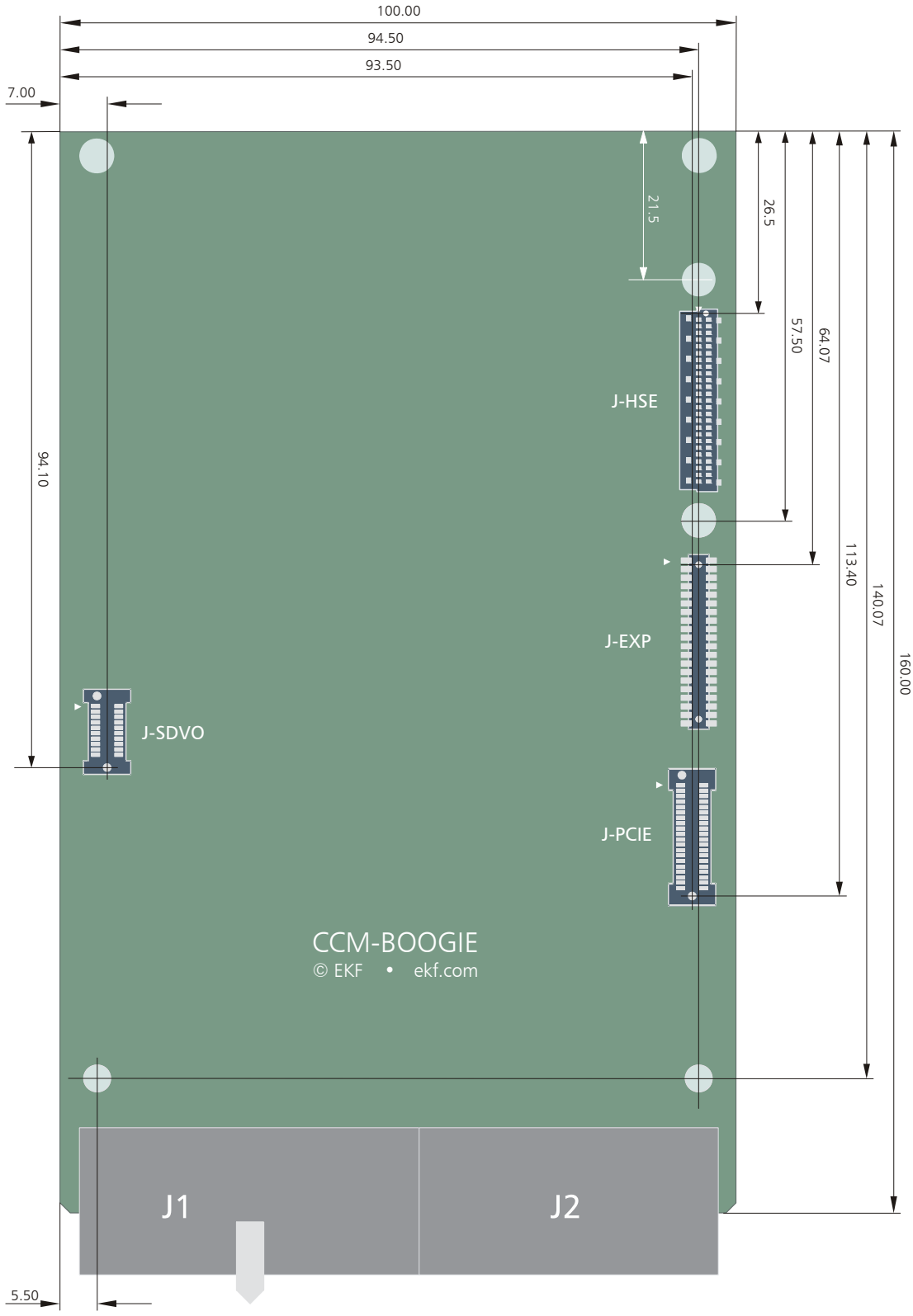
1) This pin is pulled up with 1kΩ to V(I/O). Other pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.
2) This pin is pulled up via a QuickSwitch with 2.2kΩ to +3.3V.
3) This pin is pulled up with 10kΩ to +5V.
4) This pin is protected by a resettable PolySwitch fuse.
5) This pin is not connected.
6) This pin is connected only in the rear I/O configuration.
7) This pin is pulled up with 10kΩ to +3.3V.
8) Pin positions printed blue: Rear I/O options.

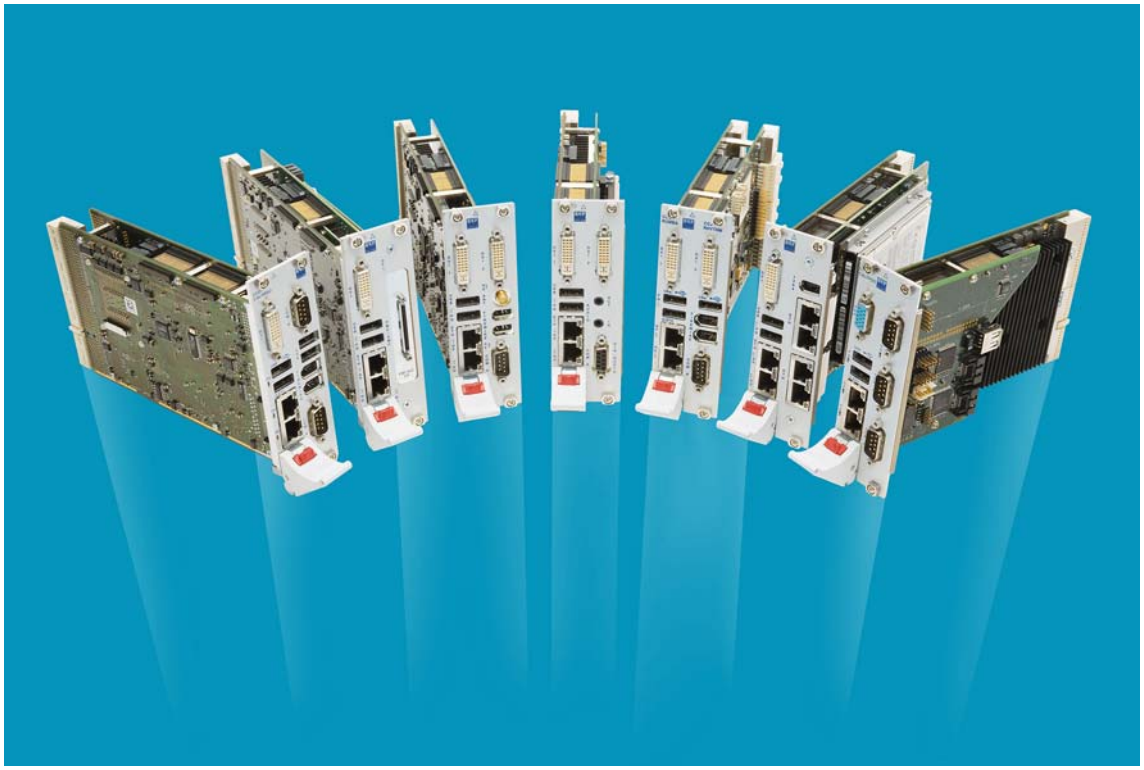


Appendix

Mechanical Drawings

The following drawing shows the positions of mounting holes and expansion connectors on the CCM-BOOGIE.





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